A new class AB differential input stage for implementation of low-voltage high slew rate op-amps and linear transconductors

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Summary

A new class AB differential stage that operates with a single supply voltage of less than two transistor threshold voltages is introduced. This circuit has utilization in high slew rate one stage op-amps, two stage op-amps with class AB input and output stages and linear transconductors. The circuit was verified with simulations and experimentally. It it is shown to have lower voltage supply requirements than other commonly used structures reported in literature.

1. Introduction

Op-amps with low supply voltage requirements, very low static power dissipation, rail-to-rail output signal swing and high slew rate are required for many applications like for delta-sigma converters used in voice and audio CODECS. One stage op-amps with class AB input stages and two stage op-amps with class AB input and output stages have several advantages:

a) Class A folded cascode op-amps have a slew rate which relates directly to the static power dissipation. High gain is achieved at the expense of cascoded output stages that cause a greatly reduced output swing, bandwidth degradation and increased noise. Two stage class AB op-amp architectures can achieve significant performance improvement with reduced static power dissipation and supply voltages.

b) Two stage op-amps with class AB output stages allow low voltage operation, rail-rail output swing (extended dynamic range) and high gain. Several efficient low-voltage class AB output stages with quiescent current control have been reported in literature recently [1]-[4]. A drawback of two stage op-amps that have a Class AB output stage and a class A input stage is that they can have high static driving capability but the class A input stage is still the limiting factor for the op-amp slew rate.

c) Two stage op-amps with Class AB input and output stages can have a very low supply voltage requirements, high slew rate and very low static power dissipation. High slew rate leads to short nonlinear settling times and allows operation at higher clock frequencies with relatively small quiescent currents (determined by the noise floor)

d) In two stage op-amps the output stage transistors have negligible contribution to op-amp noise whereas in one stage op-amps all transistors contribute to equivalent input noise.

e) If the differential pair transistors remain in saturated mode then class AB differential input stages have a linear DC transconductance characteristic. This results in reduced open loop distortion which is very important for high precision delta-sigma applications and for implementation of linear OTAs for continuous-time OTA-C applications

2. Comparison

Several efficient class AB output stages for utilization in two stage op-amps with low supply voltage requirements have been reported recently [1]-[4]. Some class AB input stages have been also reported in literature [5]-[7]. In what follows a comparison of commonly used class AB input differential stages is presented and it is shown that the new structure has lower supply requirements.

Commonly used implementations of class AB MOS differential amplifiers correspond to implementations of the same basic scheme shown in Fig. 1a. and are characterized by a class AB DC transconductance characteristic (I1,I2 vs. Vd) similar to the one shown in Fig. 2c. If both transistors remain in saturation the differential transconductance characteristic I1-I2 vs Vd is linear and the circuit can be used as a linear transconductor in OTA-C applications.

The structure of Fig. 1b was proposed in [5]. It uses "composite CMOS transistors (essentially a series combination of a PMOS and an NMOS transistor). As discussed in [6] a composite MOS

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transistor is equivalent to a regular MOS transistor with equivalent threshold voltage Vth=thN+|VthP| and transconductance gain gm=gmP gmN. This results in increased voltage supply requirements and reduced effective transconductance. In this structure the advantage of an increased slew rate is partially offset by bandwidth and noise degradation due to the reduced effective transconductance.

The structure of Fig. 1c was recently reported in [7] This structure was used in [6] for the implementation of a one stage op-amp with non cascoded output stage for delta-sigma applications. In these structures M1P and M2P operate as gain enhanced voltage followers that have create very low impedance nodes at their sources (VSA and VSB) and maintain a constant gate-source voltage (VGSQ) across their gate to source terminals. The circuit is characterized by very low static voltage supply requirements (VinQ>VGSQ+VDSsatQ) . A drawback of this circuit is that upon application of a step input differential voltage Vd=V1-V2 this voltage appears as a signal (superimposed on the quiescent value VSGQ of M1, M2) across each of the input transistors. M1 and M2: VSG1=VSGQ-Vd, VSG2=VSGQ+Vd. This increases the dynamic (transient) voltage supply requirement of the input stage to a value: Vin= VSGQ+VDSsat3+VdMAX and for matched transistors (M1,M2, and M3) the drain saturation voltage of M3 (in Fig. 1c) is given by VDSsat3=VDSsatQ+VdMAX.

The basic scheme of the new proposed structure is shown in Fig. 1d and its implementation in Fig. 1e. It operates also based on a gain enhanced (flipped) voltage follower formed by MCM and M3. This circuit generates a very low impedance node at the common source node of M1,M2 and MCM. A common mode signal detector (shown as a black box in Fig. 1e) provides a signal VCM=(V1+V2)/2 at the gate of MCM. This signal represents the common mode component of the input voltages V1 and V2. The most important characteristic of this circuit is that only one half of the differential input signal Vd appears as a signal across each of the input transistor (VSGM1=VGSQ-Vd/2 and VSGM2=VSGQ+Vd/2). This results in lower voltage supply requirements VSGQ+VDSsat3+VdMAX/2 where VDSsat3=VDSsatQ+VdMAX/2. In the case that linearity is of concern (for example for high resolution delta sigma converters and for implementation of linear transconductors) cutoff of M1 and M2 must be avoided. In this case the minimum quiescent gate-source voltage of the input devices (M1,M2 and M3) equals the maximum expected signal VSGS=Vth+VdMAX.

An advantage of the structure of Fig. 1e over that of Fig. 1c is that the quiescent voltage required to keep both input transistors active over the whole input differential range range is reduced from VSGQ=VdMAX +VTh (for the structure of Fig. 1c) to VSGQ=VdMAX/2+VTh for the structure of Fig. 1d. This allows utilization of lower bias currents. The implementation of the common mode signal detector of Fig. 1d is shown in Fig. 2a and has been reported elsewhere [8]. An even simpler implementation of the input common mode sensor uses two equal valued resistors RCM connected between both op-amp input terminals and the gate of MCM. This resistive implementation can be used only for continuous-time applications. All simulations discussed in the next section lead to essentially identical results using a resistive common mode sensor and the common mode CMOS implementation of Fig. 2a.

3. SPICE simulations

Fig. 2c shows a comparison of the simulated DC transconductance characteristics of a conventional Class A differential amplifier and of the proposed circuit of Fig. 2e. For the comparison the same bias current (Ib=0.75uA) was used. It can be seen that ,as expected, the class AB input stage has and essentially larger maximum output current.

SPICE simulations were performed to verify the performance of the proposed class AB input stage of Fig. 2b using the two stage op-amp architecture shown in Fig. 3a and the low voltage inverting configuration shown in Fig. 3b and reported in [2]. Figs. 4a and 4b show a comparison of the step transient responses for two cases: 1) a two stage op-amp with both class AB input and output stages and 2) a two stage op-amp with a class A input stage and a class AB output stage. The architecture of the op-amp is shown in Fig. 3a. Simulations were performed using the continuous-time low voltage inverting unity gain configuration shown Fig. 3b and using equal quiescent currents (the control circuit for the quiescent output current is discussed in [2]). The slew rate limiting effect of the class A input configuration can be noticed in Fig. 3b Figs. 4 and 5 show the transient currents in the input and output stages for the two cases considered above. It is clear that the op-amp with a class A input stage (and class AB output stage) can provide a relatively large static output currents but it is slew rate limited by the input stage.

All simulations were performed under following conditions: Single supply VDD=1.5V, total static current: 4uA, total static power dissipation: 6uW, bias current differential amplifier: 0.75u, transistor sizes: (M1,M2,MCM,M3): 20/1.2 Mirror loads: 40/1.2. Load and compensation capacitances:

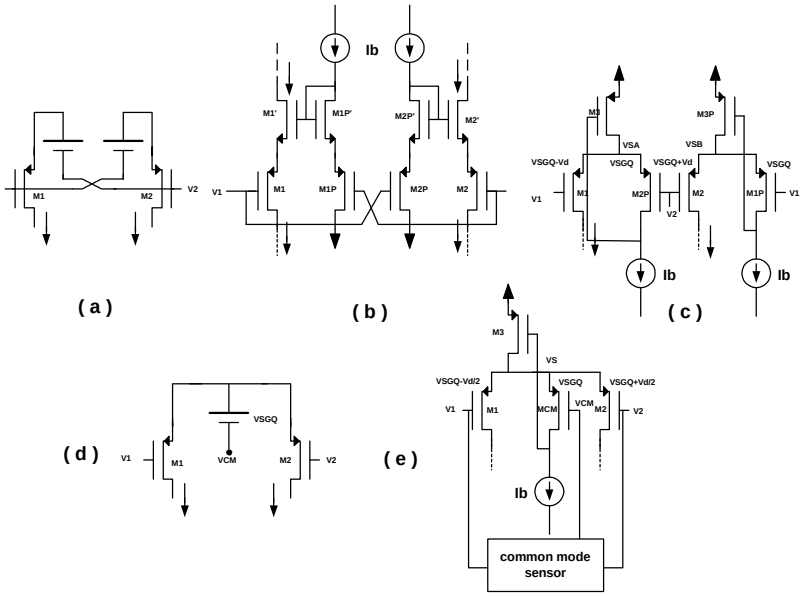

Fig. 1 Class AB input differential stages: a) Conceptual circuit type I b) Implementation in [4] c) Low voltage implementation in [5]. d) Conceptual circuit t e) Proposed implementation

0.2pF. Common mode sensing circuit: Bias current: 0.2uA, transistor sizes: 2/1.2um, Bias current output stage: 1.5uA, transistor sizes output stage MoutP: 30/2, MoutN: 20/2. Technology: 1.2 m CMOS technology parameters , transistors threshold voltages: VthN=0.45V,VthP=0.85V, BSIM Spice models.

4. Experimental results

Fig. 6 shows the experimental DC transconductance characteristic of the proposed class AB input stage. This was obtained using transistor arrays with W/L=1000/2.5 fabricated by MOSIS in 1.5um CMOS technology. 480 Ohms load resistors, a single supply voltage VDD=1.9V and a bias current Ibias=0.25mA were used.

5. Conclusions

A new class AB differential input stage with very low supply voltage requirements was introduced and verified by simulations. The proposed circuit can be used as input stage of one or two stage class AB op-amps with very high slew rate and as a linear transconductor for OTA-C applications with reduced power consumption and/or silicon area requirements.

Acknowledgements

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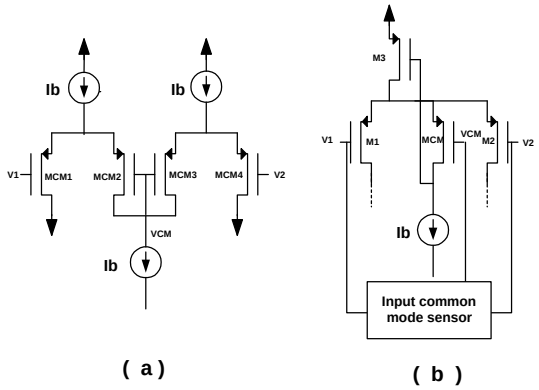
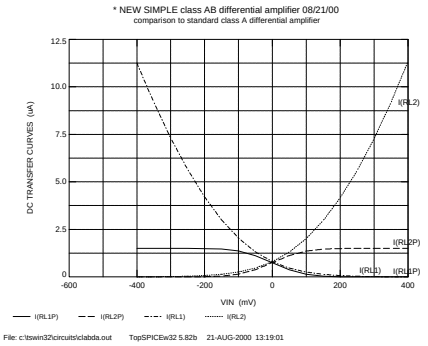
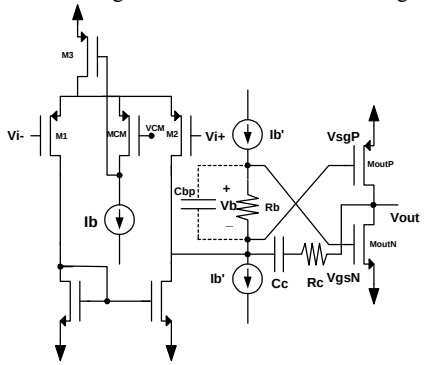


(a) (b)



(c)

Fig. 2 (a) Implementation of common mode sensing network (b) Proposed class AB input stage (c) Comparison of DC transconductance characteristics of new Class AB stage and conventional class A stage



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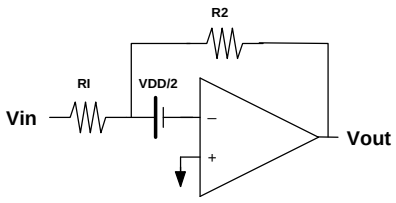
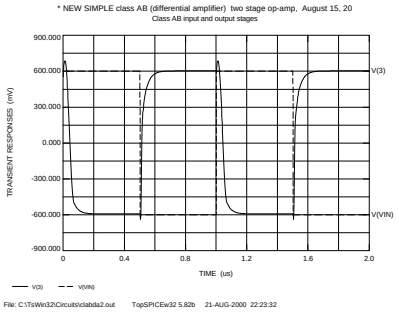
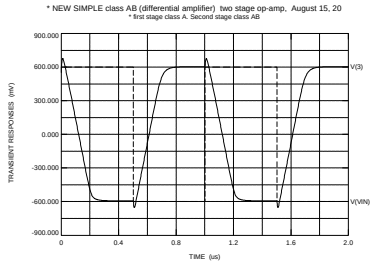


(b)

Fig. 3 (a) Low voltage two stage amplifier with class AB input and output stages (b) Low voltage test setup according to [2]



(a)



(b)

Fig. 4 Comparison of transient responses: (a) Op-amp with class AB input and output stages (b) Op-amp with class A input stage, class AB output stage

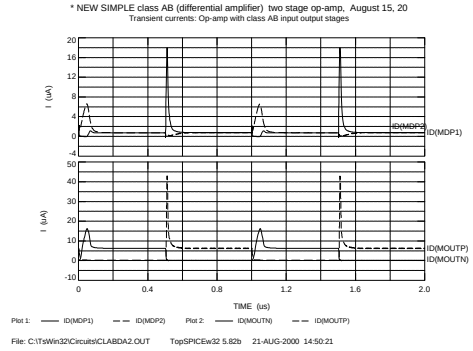


Fig. 5 Transient currents in op-amp with class AB input and output stages: Top: Transient currents in input stage Bottom: Transient current in output stage

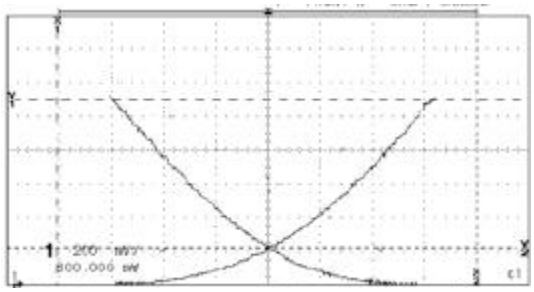


Fig. 6 Experimental transconductance characteristic of proposed class AB input stage. Vertical scale 0.2mA/div., horizontal scale: 0.15v/div.