LOW-VOLTAGE, CLASS AB AND HIGH SLEW-RATE TWO
STAGE OPERATIONAL AMPLIFIERS

BY

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ABSTRACT

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Two new low-voltage, Class-AB, two-stage operational amplifiers are proposed in this thesis project. These operational amplifiers can be operated with a single supply voltage close to a threshold voltage. The proposed operational amplifiers use a Class-AB differential stage, which provides high slew-rate. The first proposed operational amplifier uses a Class-AB output
stage with accurate quiescent current control. The second proposed operational amplifier uses a Class-AB differential amplifier as the output stage. The second proposed operational amplifier provides accurate control of the minimum current through the output transistors. Simulations are provided, which are in good agreement with expected values. Simulation comparisons between the proposed operational amplifiers and classical topologies, such as, Class-A and Class-AB (Class-A input differential pair) op-amps, are provided. The comparison proves an increased Slew-rate for the proposed topologies over the classical topologies. Experimental results are provided that are in good agreement with the simulation results.
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1 INTRODUCTION

Operational amplifiers with low-voltage supply requirements, low static power dissipation, rail-to-rail output swing and high slew-rate are desirable in applications where power dissipation efficiency is critical, such as portable electronics. Developing circuit architectures with these characteristics and implementing them in portable electronics applications will let the users enjoy their products longer before recharging or replacing the batteries.

It is shown in [Bak98] and [Joh97] that Class-A folded cascode op-amps can achieve high slew-rate. However, slew-rate for a Class-A folded cascode op-amps is directly related to its static power dissipation. Hence, a higher slew-rate in a folded cascode op-amp implies higher static power dissipation. Another feature of this architecture is that it achieves high gain by using cascoded output stages. This greatly reduces the op-amp’s output swing. High gain one-stage op-amps also use cascoded output stages thus having a reduced output swing, [Bak98] and [Joh97]. Another problem related to architectures that use cascoded output stages is that the minimum supply voltage they require is \(3V_{DSsat} + V_{TH}\), which is a high supply requirement compared to topologies available in literature that work with a minimum supply of \(2V_{DSsat} + V_{TH}\). \(V_{TH}\) is defined as the threshold voltage of the transistor device and is value is dependent on the technology used [Bak98]. \(V_{DSsat}\) is
defined as the minimum voltage present from drain to source in a MOSFET device that will keep the transistor in the saturation region [Bak98].

Two-stage op-amps with Class-AB output stages offer the advantage of high gain, high slew-rate and high rail-to-rail output swing with the advantage of low static power dissipation and low power supply. The Class-A input stage in these topologies is the limiting factor to the op-amp’s slew-rate.

Two-stage op-amps with Class-AB input and output stages offer improved slew-rate over two-stage op-amps with Class-A input and Class-AB output stages. Plus, they also provide high gain, high rail-to-rail output swing, low static power dissipation and low voltage supplies.

The purpose of this thesis work is to introduce a new two-stage architecture with Class-AB input and Class-AB output stages. This architecture operates with a minimum single voltage supply of $2V_{DSsat} + V_{TH}$. This thesis work explains the advantages of our proposed topology over Class-A input and Class-AB output stage op-amps. It also includes advantages of our proposed topology over other efficient low-voltage circuits that exist in literature.

Chapter 2 contains the basic concepts of Class-A, Class-B and Class-AB output stages. It explains why Class-AB output stage offers the best solution for power efficiency. This chapter also reviews basic topics of differential amplifiers, one-stage and two-stage operational amplifiers. Basic
concepts needed to understand the design of operational amplifiers are covered such as common mode input range, slew-rate and frequency compensation circuits. Also included in this chapter are efficient low-voltage architectures that exist in literature for Class-AB output stages and Class-AB differential amplifiers. Their advantages and disadvantages are discussed.

Chapter 3 presents the design and simulation of two new low-voltage two-stage op-amps with Class-AB input and output stages. I decided to call these architectures Full-AB op-amp and Hybrid op-amp for reasons that will be explained in detail in this chapter. Parameters such as open-loop gain, unity-gain frequency, static power dissipation and slew-rate were estimated theoretical and by simulation for the designed op-amps. A comparison between estimated and simulated results is included as well as performance comparison between our proposed topologies and Class-A op-amps and Class-A input stage, Class-AB output stage op-amps.

Chapter 4 has experimental results for a physical implementation of the circuit architectures proposed in Chapter 3. The architectures were laid out in a MOS 0.5-micron technology. Comparisons between simulated and measured results for unity-gain frequency, input-to-output transfer characteristic and slew-rate are included in this chapter. A discussion on the layout design for the fabricated circuits is also discussed in this chapter.
Chapter 5 contains a summary of the work described in detail in Chapters 2, 3 and 4. It also includes conclusions and comments on the design, simulation and testing of the proposed architectures. Recommendations for future research in this topic are also added to this chapter.
2 BASIC THEORY BEHIND OUTPUT STAGE AND OPERATIONAL AMPLIFIER DESIGN

2.1 Output Stages

The main function of an output stage is to provide a low output resistance for an amplifier. An important design requirement for an output stage is to deliver the required power level to the load in an efficient manner. This implies the power dissipated in the output stage transistors must be as low as possible. By complying with this design requirement and depending on the specific application, the output stage can help the overall circuit to prolong the life of batteries, permit smaller and lower cost power supplies, and obviate the need for cooling fans.

There exist three very well known types of output stages, Class-A, Class-B and Class-AB.

2.1.1 Class-A Output Stage

Output stages are classified according to the drain current waveform that results when an input sinusoidal signal is applied.

Figure 2.1 shows a typical drain current waveform for a transistor in a Class-A output stage. This output stage is biased at a current $I_D = 150 \mu A$, greater than the amplitude $I_d = 110 \mu A$. The transistor conducts for the entire
cycle of the input signal; thus, the conduction angle is 360°. The plot shown in Figure 2.1 is the result of simulating a Class-A output stage like the one shown in Figure 2.2. A 2kHz sinusoidal signal with 1.1 volts offset was used as the input signal in the transient analysis. The BSIM3V3 SPICE models used for the transistors are given in Appendix A.

Figure 2.1 Drain current waveforms for a Class-A output stage. A simulation was performed using circuit in Figure 2.2 and the following parameters: BSIM3V3 SPICE models (Appendix A), \((W/L)_1=100/2\), M2 source \((W/L)_2=413/6\), \(V_{DD}=2.5\) V, \(V_{SS}=-2.5\) V and \(R_L=10\) kΩ.

Classical output stage topologies that work in Class-A mode are common source and source follower configurations. The common source output stage inverts and amplifies the incoming signal. The source follower
output stage has a gain close to 1. Figure 2.2 shows a diagram of a source follower output stage.

![Diagram of a source follower Class-A output stage configuration.](image)

Figure 2.2 Source follower Class-A output stage configuration.

When there is no input signal, \( i_L \) is zero, yielding zero output voltage. However, M1 is always on and conducting an average current of \( I_D \). Because of this, the power provided by the power supply in this circuit is:

\[
P_{S(A)} = I_D \cdot (V_{DD} - V_{SS})
\]

\[(2.1.1)\]
If $V_{DD} = -V_{SS}$ then:

$$P_{S(A)} = 2*I_D^*V_{DD} \quad (2.1.2)$$

Assuming the output signal is sinusoidal with amplitude $V_o$, the average power provided to the load is:

$$P_{L(A)} = \frac{1}{2} \frac{V_o^2}{R_L} \quad (2.1.3)$$

Power efficiency is defined as:

$$\eta_A = \frac{P_L}{P_S} = \frac{V_o^2}{4*V_{DD}*R_L*I_D} \quad (2.1.4)$$

In an ideal output stage the output voltage is able to swing from the positive voltage rail to the negative voltage rail. So the following constraints occur: $V_o \leq V_{DD}$ and $V_o \leq I_D*R_L$. To understand the later condition we can refer to Figure 2.2. The maximum current that the output stage will sink is $I_D$.

Equation 2.1.4 for power efficiency can be re-written as:

$$\eta_A = \frac{1}{4} \frac{V_o}{R_L*I_D} * \frac{V_o}{V_{DD}} \quad (2.1.5)$$

Substituting the ideal output stage conditions for maximum power efficiency, that is: $V_o=V_{DD}$ and $V_o=I_D*R_L$, into equation 2.1.5 yields:
Thus, the maximum power efficiency that can be obtained for an ideal Class-A output stage is 25%.

If we use a source follower configuration (Figure 2.2) as the Class-A output stage, the maximum positive output swing is $V_{DD} - V_{GSN}$, where $V_{GSN}$ is the gate to source voltage needed to source the current $I_D$. In addition, assuming we implement the ideal current source in Figure 2.2 with a transistor, the minimum negative output swing is $V_{SS} + V_{DSsat}$, where $V_{DSsat}$ is the minimum drain to source voltage that the transistor needs to be in saturation. Transistor M1 in Figure 2.2 suffers from the bulk effect because its source is not connected to the most negative potential in the circuit ($V_{SB} \neq 0$) [Bak98]; this will make $V_{GSN}$ bigger and will degrade even more the maximum positive output swing. In Figure 2.3 a sample transfer characteristic for the source follower is shown. We used the same circuit and transistor parameters as those used in Figure 2.1. The maximum output swing as indicated in the figure is $V_{out_{MAX}} = 1.03V$ and $V_{out_{MIN}} = -2.38V$.

To estimate power efficiency using the source follower Class-A output stage, let’s consider the following conditions. The maximum undistorted output voltage is half the peak-to-peak output range, or

$$Vo = \frac{(2 \times V_{DD} - V_{DSsat} - V_{GSN})}{2} \text{ and } Vo \leq k \times I_D \times R_L,$$

where $k \leq 1$ and represents a
fraction of the maximum current $I_D$ available to the load. Substituting these new conditions in equation 2.1.5 we obtain:

$$
\eta_A = \frac{k^*}{8} \left( 2 * V_{DD} - V_{DSsat} - V_{GSN} \right) \quad (2.1.7)
$$

![Graph of Source follower Class-A output stage transfer characteristic waveform](image)

Figure 2.3 Source follower Class-A output stage transfer characteristic waveform. A simulation was performed using circuit from Figure 2.2 and the following parameters: BSIM3V3 SPICE models (Appendix A), $(W/L)_1=100/2$, M2 source $(W/L)_2=413/6$, $V_{DD}=2.5V$, $V_{SS}=-2.5V$ and $R_L=10k\Omega$.

Let us consider the next numerical example. Assume the power rails are $V_{DD} = 2.5V$ and $V_{SS} = -2.5V$. The output stage drives a $10k\Omega$ load. The bias current is $I_D = V_{DD} / R_L = 250\mu A$. Assume $V_{DSsat} = 0.25V$ and, with the
bulk effect, $V_{GSN} = 1.2V$. The actual ac current that will be delivered to the load is $i_L = (2*V_{DD} - V_{DSsat} - V_{GSN})/2*R_L = 177.5\mu A$. Therefore $k = i_L/I_D = 0.71$. Using the above results with equation 2.1.7 yields a $\eta = 0.126$. The practical implementation of a Source Follower Class-A output stage has a efficiency of 12.6%, almost half that of the theoretical maximum.

This source follower Class-A output stage is dissipating 87.4% of the power delivered by the power supply. This poor power efficiency has motivated the development of other types of output stages that can provide a better relation between the power supplied to the load and the power provided by the power supplies. Class-B and Class-AB are examples of these attempts and are reviewed below.

2.1.2 Class-B Output Stage

Figure 2.4 shows the drain current waveform for a transistor in a Class-B output stage. The transistor is biased at zero $I_D$ current and conducts for almost half the cycle of the input signal. Thus, the conduction angle is less than 180°. Because of this, the Class-B output stage needs a second transistor that will conduct in the negative half cycles. Ideally each transistor in a Class-B output stage should conduct current for half a cycle however; in practical implementations each transistor requires a small amount of input
voltage to start conducting. This effect is seen in Figure 2.4. Instead of switching directly from the positive cycle to the negative cycle, there is a small gap where the transistor is conducting zero current. This phenomenon is called crossover distortion.

![Transistor Currents (uA)](image)

Figure 2.4 Drain Current Waveforms for a Class-B Output Stage. A simulation was performed using circuit in Figure 2.5 and the following parameters: BSIM3V3 SPICE models (Appendix A), \((W/L)_1=100/2\), \((W/L)_2=300/2\), \(V_{DD}=2.5V\), \(V_{SS}=-2.5V\) and \(R_L=10k\Omega\).

Figure 2.5 shows a practical implementation for a Class-B output stage. The MOSFETS are interconnected in a source follower configuration. Transistor M1 is turned on and will conduct current during the positive cycle of the input voltage. Transistor M2 is turned on and will conduct current during
the negative cycle of the input voltage. The bias current for this circuit is zero, that is, at zero input voltage both transistors will be off and will not conduct any current. The necessary input voltages to turn on M1 and M2 is $V_{GSN}$ and $V_{SGP}$, respectively. Lets assume the input voltage starts at zero volts and is increasing. M1 will not start conducting until the input voltage reaches $V_{GSN}$. The same thing occurs when the input voltage is zero and decreasing. M2 will be off until $V_{IN}$ reaches $- V_{SGP}$. Again, this discussion helps explain crossover distortion.

Figure 2.6 shows the transfer characteristic curve for this source follower class-B output stage. In this figure we can determine the maximum output voltage swing. The threshold voltage of M1 limits the positive output swing to $V_{o+} = V_{DD} - V_{GSN}$. The threshold voltage of M2 limits the negative output swing to $V_{o-} = V_{SS} + V_{SGP}$. Transistors M1 and M2 suffer from body effect, which degrades the output swing even more. Crossover distortion is seen when $V_{IN}$ is close to zero volts.

Neglecting crossover distortion, the power delivered to the load can be written for Class-B output stages and is given by equation 2.1.8:

$$P_{L(B)} = \frac{1}{2} \frac{V_o^2}{R_L}$$ (2.1.8)
Figure 2.5 Source follower Class-B output stage

A simulation was performed using circuit in Figure 2.5 and the following parameters: BSIM3V3 SPICE models (Appendix A), $(W/L)_1=100/2$, $(W/L)_2=300/2$, $V_{DD}=2.5V$, $V_{SS}=-2.5V$ and $R_L=10k\Omega$. 

Figure 2.6 Source Follower Class-B Output Stage Transfer Characteristic Waveform. 

\begin{align*}
\text{Slope} &= 0.817 \\
\text{Slope} &= 0.85
\end{align*}
Again, neglecting crossover distortion, the current drawn from each supply consists of half sine waves of peak amplitude $V_o/R_L$. The complete average current drawn from the power supplies can be calculated with the following integral:

$$I_{S(B)} = \frac{2}{T} \int_{0}^{T/2} \frac{V_o}{R_L} \cdot \sin\left(2\pi \cdot \frac{t}{T}\right)$$

(2.1.9)

$$I_{S(B)} = \frac{1}{\pi} \cdot \frac{V_o}{R_L}$$

(2.1.10)

Total power supplied by the voltage rails is:

$$P_{S(B)} = \frac{1}{\pi} \cdot \frac{V_o}{R_L} \cdot (V_{DD} - V_{SS})$$

(2.1.11)

$$P_{S(B)} = \frac{2}{\pi} \cdot \frac{V_o}{R_L} \cdot V_{DD}$$

(2.1.12)

To find an expression for power efficiency we use equation 2.1.8 and equation 2.1.12:

$$\eta_B = \frac{P_{L(B)}}{P_{S(B)}} = \frac{\pi \cdot V_o}{4 \cdot V_{DD}}$$

(2.1.13)

For an ideal Class-B output stage the output voltage swing would be the rails, that is $V_o = V_{DD}$ or $V_{SS}$. In this case the power efficiency would be:

$$\eta_B = \frac{\pi}{4} = 0.7854$$

(2.1.14)
So the maximum efficiency obtainable for an ideal Class-B output stage is 78.54%.

If we calculate the efficiency for a practical implementation like the one shown in Figure 2.5, the maximum output swing as stated before is

\[ V_{o+} = V_{DD} - V_{GSN} \text{ or } V_{o-} = V_{SS} + V_{SGP} \]. Assuming \( V_{GSN} = V_{SGP} \), the calculated efficiency is:

\[ \eta_B = \frac{\pi}{4} \cdot \frac{V_{DD} - V_{GSN}}{V_{DD}} \tag{2.1.15} \]

Let’s assume that for a given Class-B output stage design, like the one shown in Figure 2.5, \( V_{DD} = 2.5V \) and, with the bulk effect, \( V_{GSN} = 1.2V \). Using equation 2.1.15 and the above data yields:

\[ \eta_B = 0.5027 \tag{2.1.16} \]

So the power efficiency obtained using a practical implementation for a Class-B output stage, neglecting crossover distortion, is 50.27%. This number is higher than the efficiency provided by a Class-A output stage. Even though we have a better power efficiency, we still have the crossover distortion effect that is considered unacceptable in most applications. An attempt to reduce crossover distortion is the Class-AB output stage.
2.1.3 Class-AB Output Stage

Figure 2.7 shows the drain current waveform for a transistor in a Class-AB output stage. As its name suggests, it is an intermediate solution between Class-A and Class-B output stages. This is accomplished by biasing the transistor at a non-zero dc-current that is much smaller than the peak current of the sine wave signal. Similar to Class-B, the Class-AB topology uses a second transistor that conducts in an interval slightly larger than a negative half cycle (180°). Class-AB output stages eliminate crossover distortion almost completely by maintaining both transistors at the output stage turned on. The trade-off for this attempt is to have the transistors biased at a small current. The result will be slightly lower efficiencies compared to a Class-B output stage. Figure 2.8 shows a practical implementation for a Class-AB output stage. It is very similar to the Class-B output stage configuration shown in Figure 2.5. Both MOSFET transistors are connected in a Source Follower configuration. Figure 2.8 shows the batteries \( V_{GG}/2 \) used to have both transistors, M1 and M2, on and conducting a small quiescent current. When \( V_{in} \) is zero no current will flow to the output load and M1 and M2 will have a current equal to \( Idq \). When \( V_{in} \) increases, voltage \( V_{GS1} \) will increase and M1 will start to source more current. At the same time, \( V_{GS2} \) will decrease and M2 will start to sink less current. The opposite happens when \( V_{in} \) decreases.
Figure 2.7 Drain current waveforms for a Class-AB output stage. A simulation was performed using circuit in Figure 2.8 and the following parameters: BSIM3V3 SPICE models (Appendix A), \((W/L)_1=100/2\), \((W/L)_2=300/2\), \(V_{DD}=2.5V\), \(V_{SS}=-2.5V\) and \(R_L=10k\Omega\).

Figure 2.8 shows the transfer characteristic function for a Class-AB output stage like the one shown in Figure 2.8. The transfer function shows no crossover distortion and the maximum output voltage swing is the same as the one for the source follower Class-B output stage of Figure 2.6. The maximum positive voltage swing is \(V_{O+} = V_{DD} - V_{GSN}\) and the maximum negative voltage swing is \(V_{O-} = V_{SS} + V_{GSP}\). Transistors M1 and M2 suffer from bulk effect and will degrade the output swing even more.
Figure 2.8 Source follower Class-AB output stage.

Because the Class-AB output stage is an intermediate circuit between Class-A and Class-B output stages, we can write an equation for the power given by the power supply using equation 2.1.1 and equation 2.1.12:

\[
P_{S(AB)} = 2i_{DQ}V_{DD} + \frac{2}{\pi}VoV_{DD} \quad (2.1.17)
\]

The power provided to the load, as stated before, is:

\[
P_{L(AB)} = \frac{1}{2} \frac{Vo^2}{R_L} \quad (2.1.18)
\]
The power efficiency is:

\[ \eta_{AB} = \frac{P_{L(AB)}}{P_{S(AB)}} = \frac{\pi \cdot V_o^2}{4 \cdot V_{DD} \cdot (V_o + \pi \cdot R_L \cdot I_{DQ})} \]  

\[ (2.1.19) \]

Figure 2.9 Source follower Class-AB output stage transfer characteristic waveform. 

A simulation was performed using circuit in Figure 2.8 and the following parameters: BSIM3V3 SPICE models (Appendix A), \((W/L)_1=100/2, (W/L)_2=300/2, V_{DD}=2.5V, V_{SS}=-2.5V\) and \(R_L=10k\Omega\).

For an ideal Class-AB output stage, the output voltage may swing all the way to the positive or negative rails, \(V_{DD}\) or \(V_{SS}\). Another condition valid for the ideal case is \(I_{DQ} = 0\). Equation 2.1.19 reduces to equation 2.1.14, yielding the same maximum efficiency as the Class-B output stage. 78.54% of the total power is delivered to the load.
Let’s assume a practical case, similar to the one proposed for the Class-B output stage. Voltages $V_{DD} = 2.5\,V$ and $V_{GSN} = 1.2\,V$ (including bulk effect). Let’s assume we have a load $R_L$ of $20\,k\Omega$. This load determines the maximum current that the output stage should source or sink. In this case $I_{max} = V_{DD}/R_L = 125\,\mu A$ however, the maximum current will also be determined by the maximum output voltage swing $V_{o+} = V_{DD} - V_{GSN} = 1.3\,V$.

The maximum current is therefore $I_{max_{AB}} = 1.3\,V/20\,k\Omega = 65\,\mu A$. Let’s assume the output MOSFET transistors are biased to have a quiescent current that is the 10% of the maximum current, that is $I_{DQ} = 6.5\,\mu A$. With these data, the maximum power efficiency is calculated to be:

$$\eta_{AB} = \frac{\pi^* (V_{DD} - V_{GSN})^2}{4 \pi^* V_{DD} (V_{DD} - V_{GSN} + \pi^* R_L^* I_{DQ})}$$

(2.1.20)

$$\eta_{AB} = \frac{\pi^* 1.3V^2}{4 \pi^* 2.5(1.3V + \pi^* 20k\Omega \times 6.5\,\mu A)} = 0.311$$

(2.1.21)

Result (2.1.21) indicates that 31.1% of the total power is provided to the load. Efficiency is inversely dependent on quiescent current so the smaller we can make this current, the better.

Several ways to implement the floating batteries required for a Class-AB output stage exist in the literature. One of these implementations is shown in Figure 2.10 [Bak98]. The gate of M6 is biased at a DC-voltage so that its
drain current is equal to the current set by M3. Transistor M3 is just a current source. The drain to source voltage of M4 and M5 are constant because the current that flows through them is constant. These voltages are also the biasing voltages for transistors M1 and M2.

The gain provided by the output stage in Figure 2.10 can be estimated by looking at the small signal model shown in Figure 2.11.

\[
Av = \frac{V_{out}}{V_{in}} = -\frac{gm6}{(\frac{1}{ro} + \frac{1}{ro6})} 
\]  

(2.1.22)

The terms \(1/gm5\) and \(1/gm4\) were omitted in equation 2.1.22 because they are small in comparison to \(ro3\).

Figure 2.10  Practical implementation of a Class-AB output stage.
A scheme used for low voltage applications is shown in Figure 2.11 [Bak98]. The reason for its extensive use in low-voltage applications comes from the fact that the output has a rail-to-rail swing capability. Rail-to-rail output swing is defined as a voltage that can swing within $V_{DS_{sat}}$ of the voltage rails, $V_{o+} = V_{DD} - V_{DS_{sat}}$ and $V_{o-} = V_{SS} + V_{DS_{sat}}$. Transistors M1 and M2 are interconnected in a common-source configuration. Because of this, the output stage has a gain of $A = -(gm1 + gm2) * R_{out}$. Current $i_{in}$ in this figure may be flowing into the circuit or may be flowing out. If it is flowing in, the current of M4 will decrease in order to preserve the relation $I = i_{in} + i_{D4}$. This will
decrease $V_{GS4}$ and $V_{GS1}$ and therefore $i_{D1}$ will decrease. At the same time the current across M3 will increase satisfying the relation $i_{D3} = I + i_{in}$ . This will increase $V_{GS3}$, $V_{GS2}$ and finally $i_{D1}$ will increase.

![Class-AB output stage using floating current source.](image)

Figure 2.12 Class-AB output stage using floating current source.

The gain of configuration shown in Figure 2.12 is estimated by looking at the small signal model of Figure 2.13. The gain is:

$$
Av = \frac{V_{out}}{V_{in}} = -(g_{m2} + g_{m1})(r_{o2} || r_{o1})
$$

(2.1.23)
The small-signal output resistance is estimated by:

\[
R_{out} = (ro_2 || ro_1)
\]  

(2.1.24)

\[\text{Figure 2.13 Small-Signal Model for Figure 2.12.}\]

A variety of Class-AB output stages exist in literature. A review of some of these configurations is presented in the following subsections.

2.1.3.1 Class-AB Output Stage Based on a Complementary Head to Tail Connected Transistors

The output stage shown in Figure 2.14 is presented in [Lan98] and reviewed in [Was99]. The configuration is based on a floating battery, \(V_{AB}\), implemented by two complementary head-to-tail connected transistors M9 and M10 and biasing transistors M3 to M6. Current \(I_{in}\) may be flowing into the node or may be flowing out of the node. This current represents the output of
a differential pair that constitutes the input stage of a two stage operational amplifier. The differential pair and the two stage operational amplifiers are reviewed in sections 2.2.1 and 2.2.5, respectively.

Transistors M4 and M5 are sized twice the sizes of transistors M9 and M10, respectively. Transistors M9 and M10 are sized equal to transistors M3 and M6 respectively.

Under quiescent conditions the drain current through transistor M9 or M10 will be \( I_B/2 \) and their respective gate-to-source voltages will be equal to the gate-to-source voltages of transistors M4 and M5. This situation will make the gate-to-source voltages of output transistors M1 and M2 equal to the gate-to-source voltages of transistors M6 and M3 respectively. If the output transistors M1 and M2 are sized \( n \) times the sizes of transistors M6 and M3 respectively, then the output transistors quiescent current is \( n \cdot I_B \).

If a current \( I_{in} \) flows into node X, the voltage at that node will increase and at the same time the voltage at node Y will also increase. This situation will decrease \( V_{GS9} \) sinking less drain current. Transistor M10 will source more current and its \( V_{GS10} \) will increase pulling up node W. The increase in voltage at node Y will increase \( V_{GS2} \) and transistor M2 will sink current from the output node. The increase in voltage at node W will decrease \( V_{GS1} \) making transistor M1 source less current. The output stage will be sinking current from the output node. The opposite case happens when current \( I_{in} \) flows out of node X,
the gate-to-source voltage of transistor M2 decreases while the gate-to-
source voltage of transistor M1 increases. Hence, the output stage sources
current to the output node.

When a large gate-to-source voltage drives one of the output
transistors (either M1 or M2), the other output transistor is held at a minimum
gate-to-source voltage clamped by the control transistors M9 or M10. This
will leave a minimum drain current flowing through the inactive transistor.
This configuration prevents the output transistors from cutting off.

The disadvantage of the circuit shown in Figure 2.14 is that the
minimum supply voltage is equal to two gate-to-source voltages and one
saturation voltage.

2.1.3.2 Low-Voltage Class-AB Buffers with Quiescent Current Control

The Class-AB output stage design presented in [You98] introduces a
topology with quiescent current control. The quiescent current in the output
stage is not sensitive to process variations. The topology introduced in
[You98] is based on a Class-AB output stage circuit shown in Figure 2.15.

When \( V_{IN} \) increases, both transistors M1 and M2 sink more current and
transistor M3 will source more current while transistor M4 will sink less
current. The gate-to-source voltage of transistor M3 will increase and will
drive transistor Moutp to source current to the output node. The opposite happens when $V_{\text{IN}}$ decreases. Both transistors M1 and M2 will sink less current causing transistor M3 to source less current while M4 sinks more current. The increase in the gate-to-source voltage of transistor M4 will drive output transistor Moutn to sink current from the output node.

Figure 2.14 Output stage based on a complementary head-to-tail connected transistors [Lan98].

Under quiescent conditions, transistors M3 and M4 are designed to source and sink a current $a \times I_B$. If output transistors Moutp and Moutn are
sized to be \( n \) times the size of transistors M3 and M4, the output stage quiescent current is \( n \times a \times I_B \). The low sensitivity to process variations of the circuit in Figure 2.15 is due to the reduced gain of the intermediate inverting amplifier stages which are loaded by diode connected transistors, M3 and M4. However, the gain reduction weakens the drive required by Moutp and Moutn.

To solve the problem of low gain of the circuit shown in Figure 2.15, a new circuit configuration is proposed in [You98] and it features an adaptive load. The configuration is shown in Figure 2.16.

![Figure 2.15 Output stage using diode-connected transistors to control the quiescent current](image-url)
Under quiescent conditions, transistors M5 to M8 are in saturation and the loading at nodes A and B is small. Transistors M6/M8/Moutn and M5/M7/Moutp are current mirrors respectively. The quiescent output current is set to \( n \times a \times I_B \).

If \( V_{IN} \) increases, transistor M1 pulls more current from transistors M5 and M7. The gate-to-source voltage of transistor M7 increases pulling down the voltage at node A. At the same time, the gate-to-source voltage of transistor M5 increases pulling up the voltage at node S. Transistor M7 enters the linear region. Therefore, node A becomes loaded at a higher resistance.

If \( V_{IN} \) decreases, transistor M2 pulls less current provided by transistor M4 and more current will flow through transistors M6 and M8. The gate-to-source voltage of transistor M8 increases pulling up the voltage at node B. The gate-to-source voltage of transistor M6 increases pulling down the voltage at node P. Transistor M8 enters the linear region. Therefore, node B becomes loaded at a higher resistance.

The important features introduced by the topology proposed in [You98] and shown in Figure 2.16 is the capability to achieve control over quiescent current without sacrificing current drive in Class-B mode. However, a disadvantage is that the dependence on process variations is not fully
eliminated.

### 2.1.3.3 Low-Voltage Feedback Class-AB Output Stage with Minimum Selector

A topology proposed in [Lan98] is shown in Figure 2.17. This implementation uses a minimum selector circuit constituted by transistors M5 to M7. A minimum selector circuit controls the quiescent current of the output transistors, Moutp and Moutn. It also maintains a minimum current on the inactive output transistor when the other output transistor is driven hard.
Figure 2.16 Output stage using an adaptive load configuration to control the quiescent current [You98].

Transistor M6 of the minimum selector circuit operates mainly on triode region. Only when output transistor Moutp has a large gate-to-source voltage does transistor M6 enter saturation region. The drain current of transistor M5 flows through transistor M4 and steers the differential amplifier constituted by M1 and M2. This Class-AB signal differential amplifier will regulate the gate voltages of transistors Moutp and Moutn to make the current that flows through transistor M4 equal to $I_{ref}$. 
Under quiescent conditions, transistors M5 to M7 are designed to have the same gate-to-source voltages. Because M6 is in the triode region, the combination of transistors M5/M6 can be considered as one transistor with double the length. With this situation, the current that flows through transistor M4 will be half the current that flows through transistors M7 and M8. The Class-AB signal differential amplifier (M1/M2) will make the drain current of transistor M4 equal to $I_{\text{ref}}$. Therefore the quiescent output current is:

$$I_{\text{Q}} = \frac{2 \times W_{\text{outn}} \times L_{8}}{L_{\text{outn}} \times W_{8}} \times I_{\text{ref}} \tag{2.1.25}$$

When transistor Moutp sources a large current, its gate-to-source voltage will be large. In this situation, transistor M6 will be in saturation mode. The set of transistors M5 to M7 will be operating as a cascoded current mirror. The current of transistor Moutn is regulated to be equal to half the quiescent current.

$$I_{\text{Doutn}} = \frac{W_{\text{outn}} \times L_{8}}{L_{\text{outn}} \times W_{8}} \times I_{\text{ref}} \tag{2.1.26}$$

When transistor Moutn sinks a large current, a large current will also flow through transistors M8 and M7. Transistor M6 will pull the source of transistor M5 to the positive voltage supply. Transistors M5 and Moutp will form a current mirror. As a result, a replica of Moutn drain current will flow through transistor M4. The Class-AB signal differential amplifier will force the
current through M4 to be equal to $I_{ref}$ and the minimum Moutp drain current will be set equal to:

$$I_{D_{outp}} = \frac{W_{outp} \cdot L_5 \cdot I_{ref}}{L_{outp} \cdot W_5}$$  \hspace{1cm} (2.1.27)

If transistors Moutp and M5 are sized equal to Moutn and M8 respectively, the minimum current of the inactive output stage transistor is set to:

$$I_{MIN} = \frac{W_{outp} \cdot L_5 \cdot I_{ref}}{L_{outp} \cdot W_5} = \frac{W_{outn} \cdot L_8 \cdot I_{ref}}{L_{outn} \cdot W_8}$$  \hspace{1cm} (2.1.28)

The advantage of the topology shown in Figure 2.17 is that the output transistors never cut off and are biased at a minimum drain current. The disadvantages are: (1) the minimum supply voltage must be equal to two drain-to-source saturation voltages plus a gate-to-source voltage and (2) careful circuit design and frequency compensation is needed due to the Class-AB feedback quiescent current control.
2.2 Operational Amplifiers

The operational amplifier (op-amp) is a fundamental building block in analog integrated design and is used to realize functions ranging from dc bias generation to high-speed amplification or filtering. Many configurations for op-amps exist in the literature. Two classifications that encompass most of the
existent topologies are one-stage and two-stage op-amps. By reasons that will become evident later on in this explanation, two–stage op-amp topologies are the best choice for low voltage applications. In Figure 2.18 a block diagram for a two-stage op-amp is shown.

Before continuing talking about operational amplifiers, a brief section that explains the basic features of differential amplifiers is provided.

![Figure 2.18 Block diagram for a two-stage op-amp.](image)

2.2.1 Differential Amplifiers

The basic building block in an op-amp circuit is the differential amplifier like the one shown in Figure 2.19. A differential amplifier will only amplify a differential signal between its inputs while it will suppress common mode signals. When both inputs of the differential amplifier are equal, a current
\( I_{ss}/2 \) will flow through M1 and M2, satisfying the relation \( I_{SS} = i_{D1} + i_{D2} \).

![Differential amplifier diagram](image)

Figure 2.19 Differential amplifier.

To understand the functionality of the differential amplifier, let’s assume \( v_{in1} - v_{in2} \) can vary from \( V_{DD} \) to \( V_{SS} \). If \( v_{in1} \) is much more negative than \( v_{in2} \), M1 is off with zero \( i_{D1} \) current, M2 has a current \( i_{D2} = I_{SS} \). Voltage \( v_{OUT1} \) is equal to \( V_{DD} \) while \( v_{OUT2} \) is equal to \( V_{DD} - I_{SS} \cdot R_{D} \). If \( v_{in1} \) is brought closer to \( v_{in2} \) then M1 turn on having a nonzero current \( i_{D1} \), again satisfying \( I_{SS} = i_{D1} + i_{D2} \). If \( v_{in1} \) is much more positive than \( v_{in2} \), then all current \( I_{SS} \) will flow through transistor M1 while M2 will be off. Figure 2.20 shows the transfer
characteristics for the circuit in Figure 2.19.

Figure 2.20 DC transfer characteristic function: a) output voltages of differential amplifier shown in Figure 2.19. b) Differential output voltage for differential amplifier shown in Figure 2.19. A simulation was performed using Figure 2.19 and the following parameters: BSIM3V3 SPICE models (Appendix A), $(W/L)_1=17/6$, $I_{SS}=20\mu A$, $V_{DD}=2.5V$, $V_{SS}=-2.5V$ and $R_{D1}=R_{D2}=150k\Omega$.

To quantify the behavior of the MOS differential pair, the relation between the currents $i_{D1}$ and $i_{D2}$ with respect to $vid = v_{in1} - v_{in2}$ can be found as shown below. Two equations can be written for $i_{D1}$ and $i_{D2}$ assuming saturation:

$$i_{D1} = \frac{1}{2} KPn^+ W \left( \frac{V_{GS1} - V_{THN}}{L} \right)^2$$  \hspace{1cm} (2.2.1)
Equations 2.2.1 and 2.2.2 can be rewritten as:

\[ i_{D1} = \sqrt{\frac{1}{2} KPN \frac{W}{L} (V_{GS1} - V_{THN})^2} \]  

(2.2.3)

\[ i_{D2} = \sqrt{\frac{1}{2} KPN \frac{W}{L} (V_{GS2} - V_{THN})^2} \]  

(2.2.4)

Subtracting equation 2.2.3 minus equation 2.2.4 and using \( V_{GS1} - V_{GS2} = \text{Vid} \)

\[ \sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2} KPN \frac{W}{L} \text{Vid}} \]  

(2.2.5)

Using equation \( I_{SS} = i_{D1} + i_{D2} \) and equation 2.2.5 and solving for \( i_{D1} \) and \( i_{D2} \):

\[ i_{D1} = \frac{I_{SS}}{2} + \frac{KPN \frac{W}{L} I_{SS} \left( \frac{\text{Vid}}{2} \right)}{1 - \frac{(\text{Vid}/2)^2}{\left( I_{SS}/KPN \frac{W}{L} \right)}} \]  

(2.2.6)

\[ i_{D2} = \frac{I_{SS}}{2} - \frac{KPN \frac{W}{L} I_{SS} \left( \frac{\text{Vid}}{2} \right)}{1 - \frac{(\text{Vid}/2)^2}{\left( I_{SS}/KPN \frac{W}{L} \right)}} \]  

(2.2.7)

When \( \text{Vid} = 0 \), then
\[ i_{D1} = i_{D2} = \frac{I_{SS}}{2} \]  
\[ V_{GS1} = V_{GS2} = V_{GS} \]  

And consequently,

\[ \frac{I_{SS}}{2} = Kp n \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})^2 \]  

If we substitute equations 2.2.8, 2.2.9 and 2.2.10 into equations 2.2.6 and 2.2.7 we can obtain:

\[ i_{D1} = \frac{I_{SS}}{2} + \left( \frac{I_{SS}}{V_{GS} - V_{THN}} \right) \cdot \left( \frac{vid}{2} \right) \cdot \sqrt{1 - \left( \frac{vid/2}{V_{GS} - V_{THN}} \right)^2} \]  
\[ i_{D2} = \frac{I_{SS}}{2} - \left( \frac{I_{SS}}{V_{GS} - V_{THN}} \right) \cdot \left( \frac{vid}{2} \right) \cdot \sqrt{1 - \left( \frac{vid/2}{V_{GS} - V_{THN}} \right)^2} \]  

For \( vid/2 \ll V_{GS} - V_{THN} \), the small-signal approximation, we can rewrite equations 2.2.11 and 2.2.12 as:

\[ i_{D1} = \frac{I_{SS}}{2} + \left( \frac{I_{SS}}{V_{GS} - V_{THN}} \right) \cdot \left( \frac{vid}{2} \right) \]  
\[ i_{D2} = \frac{I_{SS}}{2} - \left( \frac{I_{SS}}{V_{GS} - V_{THN}} \right) \cdot \left( \frac{vid}{2} \right) \]  

As stated in [Bak98], a MOSFET transistor biased at a certain \( I_D \) has
\[ gm = \frac{2^*I_D}{(V_{GS} - V_{THN})} \]. For MOSFETS M1 and M2 we have:

\[ gm_{1,2} = \frac{2^* \left( \frac{I_{SS}}{2} \right)}{(V_{GS} - V_{THN})} = \frac{I_{SS}}{(V_{GS} - V_{THN})} \] \hspace{1cm} (2.2.15)

With equations 2.2.13, 2.2.14 and 2.2.15 it is evident that as \( vid \) increases, the current at M1 increases as the current in M2 decreases. The small signal current is:

\[ i_d = gm^* \frac{vid}{2} \] \hspace{1cm} (2.2.16)

Figure 2.21 shows a plot of \( i_{D1}, i_{D2} \) vs. \( vid \). This figure was obtained from a simulation of the schematic shown in Figure 2.19. As can be seen in the figure, when one of the currents, either \( i_{D1} \) or \( i_{D2} \) goes to \( I_{SS} \), the other goes to zero.

2.2.2 Common-Mode Input Range (CMR)

An important issue concerning differential amplifiers is their input common-mode range (CMR). This is a range of voltages common to both input gates that maintain all the transistors in the differential amplifier in the saturation mode. Figure 2.22 helps us do the input CMR analysis.
Figure 2.21 Drain currents in a differential amplifier. A simulation was performed using circuit in Figure 2.19 and the following parameters: BSIM3V3 SPICE models (Appendix A), \((W/L)_{1}=17/6\), \(I_{SS}=20\mu A\), \(V_{DD}=2.5V\), \(V_{SS}=-2.5V\) and \(R_{D1}=R_{D2}=150k\Omega\).

The minimum common-mode input voltage can be calculated by noticing that M6 requires a \(V_{DSsat}\) to be in saturation. Also M1 requires a voltage \(V_{GS}\) that surpasses the threshold voltage.

\[
v_{1\ min} = V_{GS1} + V_{DSsat6} + V_{SS} = \sqrt{\frac{I_{SS}}{\beta_1}} + V_{thn} + \sqrt{\frac{2\cdot I_{SS}}{\beta_6}} + V_{SS} \tag{2.2.17}
\]
Figure 2.22 Differential amplifier with both inputs tied to the same voltage.

The maximum common-mode input voltage can be calculated by noticing that M1 and M2 may enter triode region. This occurs when:

\[
V_{DS1} = V_{GS1} - V_{THN} \Rightarrow V_{D1} = V_{G1} - V_{THN} \Rightarrow V_{G1} = V_{D1} + V_{THN}
\]  

(2.2.18)

Since \( V_{G1} = v_i \text{ max} \) then,
\[ v_{I, \text{max}} = V_{DD} - V_{GS3} + V_{GD1} = V_{DD} - \left[ \frac{I_{SS}}{\beta_3} + V_{THP} \right] + V_{THN} \] (2.2.19)

So the input common-mode (CMR) is delimited by a positive CMR = \( v_{I, \text{max}} \) and a negative CMR = \( v_{I, \text{min}} \).

### 2.2.3 Small-Signal Gain for a Differential Amplifier

To determine the small signal gain, let's consider the input differential voltage given by,

\[ v_{i1} = v_{gs1} - v_{gs2} = i_{d1}^* \frac{1}{gm1} - i_{d2}^* \frac{1}{gm2} \] (2.2.20)

Ideally zero current flows through M6 so,

\[ i_{d1} = -i_{d2} = i_d \text{ and } gm1 = gm2 = gm \] (2.2.21)

Taking this into consideration in equation 2.2.20 yields

\[ v_{i1} = id^* \frac{2}{gm} \] (2.2.22)

In Figure 2.23 a differential pair with the respective AC currents is shown. When \( v_{i1} \) goes higher than zero, the overall current \( i_{D1} \) is going to increase by a small signal differential current while the overall current \( i_{D2} \) decreases by the same amount if and only if equations 2.2.21 holds. This can be seen as a small signal current \( i_d \) flowing out of the drain of M2. This is
shown in Figure 2.23. The same \( i_d \) is added to \( i_{d1} \) and copied by transistor M3 to transistor M4. The overall small signal current at the output node will be two times \( i_d \). The resistance looking into the drain of M4 is:

\[
ro4 = \frac{1}{\lambda I_D} \tag{2.2.23}
\]

The resistance looking into the drain of M2 is:

\[
R_{int_{D2}} = ro2^*\left(1 + gm2^* \frac{1}{gm1}\right) \approx ro2 \tag{2.2.24}
\]

![Differential pair showing AC currents](image)

Figure 2.23 Differential pair showing AC currents.

The output impedance is then:

\[
R_{out} = ro2 || ro4 \tag{2.2.25}
\]
The output voltage is:

\[ V_{out} = 2^{*}i^{d}^{*}R_{out} \]  \hspace{1cm} (2.2.26)

The voltage gain is:

\[ A_{V} = \frac{V_{out}}{V_{i1}} = \frac{V_{out}}{V_{i1} - V_{i2}} = \frac{2^{*}i^{d}^{*}(r_{o2}||r_{o4})}{i^{d}^{*} \frac{2}{g_{m}}} = g_{m}^{*}(r_{o2}||r_{o4}) \]  \hspace{1cm} (2.2.27)

### 2.2.4 Slew Rate in a Differential Amplifier

An important nonlinear effect that is present in any circuit that includes capacitive loads is called slew rate. The slew rate is the maximum rate of change of the output voltage of a circuit in response to a change in the input signal. This is seen in Figure 2.24 where the output of a differential pair is driving a capacitive load. The maximum current that the differential pair can source or sink is \( I_{SS} \). The voltage at load capacitance \( C_{L} \) is:

\[ V_{L} = \frac{Q}{C_{L}} \]  \hspace{1cm} (2.2.28)

Were \( Q \) is the charge stored in the capacitor. If we take the derivative of equations 2.2.28 with respect to time, the result will provide the output voltage rate of change:
\[
\frac{dV_L}{dt} = \frac{1}{C_L} \cdot \frac{dQ}{dt} = \frac{I_L}{C_L}
\]  \hspace{1cm} (2.2.29)

For \(I_{L\text{max}} = I_{SS}\), slew rate is:

\[
SR = \frac{I_{SS}}{C_L}
\]  \hspace{1cm} (2.2.30)

Figure 2.24 Slew-rate limitations on differential amplifiers.

Slew rate is measured in \(V/\mu s\). Let’s assume we have a differential pair with tail current \(I_{SS} = 1mA\). The differential pair is driving a capacitive load of \(C_L = 20pF\). The slew-rate for this differential pair is
SR = 1mA/20pF = 50V/μs. If the input signals to the differential pair changes faster than its slew rate, the output will not be able to follow it. A simulation was performed to illustrate the slew rate non-linearity. A voltage follower configuration, Figure 2.24, was used. The gate of transistor M6 was biased for its drain current, \( I_{ss} = 1mA \). The circuit is tested with an input signal, \( v_{i1} \), of 1 volt peak, 2Mhz, squared signal centered at 0 volts. The circuit is loaded with a 20pF capacitor. As mentioned above, the slew rate limitation under these conditions is 50V/μs. Figure 2.25 shows the input and corresponding output signal. From the plot it is seen that the input signal changes from –1 V to 1 V at a rate of 200V/μs. This rate is four times bigger than the slew rate of the differential amplifier used in the voltage follower configuration. It is evident from the plot that the output signal takes some time to change from -1V to 1 V or 1 V to -1 V trying to follow the change at the input.

2.2.5 Two-Stage Op-Amp

A basic two-stage op-amp schematic is shown in Figure 2.26. Compared to Figure 2.18, the different blocks can be distinguished in the schematic. Transistors M1-M4 implement the differential amplifier; transistors M7-M8 are the realization of a common-source output stage. The current established by transistor M5 is copied into transistor M6 and M8.
Let’s assume we have a positive $\text{vid} = v_{i1} - v_{i2}$. The voltage at the output of the differential pair (drain of M2 and M4) increases. This will decrease the voltage from gate to source of M7 and will start shutting it off. The M7 drain voltage will decrease, sourcing less current. Transistor M8 will pull current from the output node. If vid decreases, the opposite will happen. The differential output voltage decreases turning on transistor M7. This will cause M7 drain voltage to increase, sourcing more current to the output node.
Recalling equations 2.2.25 and 2.1.23 we can obtain the open loop gain of the two-stage op-amp shown in Figure 2.26.

\[
A_{OL} = gm_1*(ro_2||ro_4)^*[-gm_7*(ro_7||ro_8)]
\] (2.2.31)

### 2.2.6 Compensating a Two-Stage Op-Amp

Before going into detail about compensating two-stage op-amps, we need to define feedback. Feedback is combining the output signal with the input signal of a system and inputting the result to the system itself. There are a lot of examples in practice where feedback is applied. For example, a thermostat of an air conditioner uses feedback to maintain the temperature in...
a room constant. A sensor in a tank, which indicates when the tank is full, may control a water gate that will maintain the tank full. Even we use negative feedback. For example, when we take a bath, our skin senses the water temperature and sends a signal to our brain that will help decide whether we adjust the water temperature or leave it as it is.

There are two types of feedback. Negative feedback is when the output is subtracted from the input and the result is input to the system. Negative feedback stabilizes a system. Positive feedback is when the output is added to the input. Positive feedback makes a system become unstable [Bak98]. The three examples mentioned above utilize negative feedback. An example of positive feedback is when a microphone is put close to the speaker. A sound detected by the microphone will be amplified and the output of the speaker will produce an audible sound that will feed back to the microphone. This cycle will create a loud and annoying noise. In some electronic systems, positive feedback can be used in a controlled manner to implement such useful circuits as oscillators.

In most applications where op-amps are used, negative feedback is applied. The use of negative feedback has many good features like, (1) it desensitizes gain to temperature, mismatch of devices or any other parameters, (2) it increases the usable bandwidth of the op-amp, (3) it reduces nonlinear effects inherently present in op-amps and (4) it increases
the input resistance and decreases the output resistance of the op-amp. For a
detailed explanation of these features refer to [Bak98].

In Figure 2.27 a block diagram of a system using negative feedback is
shown. The following equations may be written:

\[
vo = xi * A_{OL}(jw) \tag{2.2.32}
\]

\[
xi = vi - xf \tag{2.2.33}
\]

\[
xf = \beta * vo \tag{2.2.34}
\]

Using the above equations to solve for \(\frac{vo}{vi}\), also known as the closed
loop gain,

\[
A_{CL}(jw) = \frac{vo}{vi} = \frac{A_{OL}(jw)}{1 + \beta * A_{OL}(jw)} \tag{2.2.35}
\]

In equation 2.2.35, the open loop gain, \(A_{OL}\), is generally in the order of
thousands. If the denominator can be approximated as

\[
1 + \beta * A_{OL}(jw) \approx \beta * A_{OL}(jw), \quad \text{equation 2.2.35 becomes:}
\]

\[
A_{CL} \approx \frac{1}{\beta} \tag{2.2.36}
\]

The closed loop gain, \(A_{CL}\), depends only on the feedback factor \(\beta\). An
example of an op-amp connected with feedback with \(\beta = 1\) is shown in Figure
2.28. This configuration is commonly known as voltage follower.
A problem that comes with any type of feedback is that the system becomes susceptible to instability. When negative feedback is applied, a phase shift in the output signal may cause the negative feedback to become positive feedback.

Figure 2.27 Negative feedback model.

A problem that comes with any type of feedback is that the system becomes susceptible to instability. When negative feedback is applied, a phase shift in the output signal may cause the negative feedback to become positive feedback.

Figure 2.28 Voltage follower configuration.
To analyze the instability problem let’s calculate the loop gain from Figure 2.27:

\[ A_{FB} = \frac{x_f}{x_i} = \beta^* A_{OL}(jw) \]  

(2.2.37)

If the change in phase of \( A_{FB} \) is 180° and its magnitude is less than unity, or 0dB, the system will be stable [Bak98]. If the change in phase of \( A_{FB} \) is 180° and its magnitude is greater than 0dB, the system is unstable [Bak98].

There are two parameters helpful in the determination of stability for a system. Phase margin, \( PM \), is the number of degrees in phase above -180° when the system is operating at a gain of 0dB. A rule of thumb is \( 45° \leq PM \leq 90° \) [Bak98]. The optimum value for phase margin is 60°, [Bak98]. The second parameter is called gain margin, \( GM \), and is the number of dB’s in gain below 0dB at the frequency were the phase is -180°. A rule of thumb is \( GM \geq 10dB \) [Bak98].

Two–stage op-amps have two high impedance nodes. Those high impedance nodes are located at the output of the first stage (drains of M4 and M2 in Figure 2.26) and the output of the second stage. These high impedance nodes will create the dominant pole and the 2nd dominant pole of the system. If these two poles are close to each other, the system is at risk of becoming
A simulation of a two-stage op-amp was performed to illustrate its frequency response. The two-stage op-amp used is that shown in Figure 2.26, but without the compensation capacitor, $C_C$. The circuit configuration to obtain the open loop gain and phase against frequency is shown in Figure 2.29. The resistance in this configuration is used to ensure stable DC operation. The capacitance with the resistance creates a very low frequency pole that eliminates AC signal feedback to the negative input of the op-amp. Figure 2.30 shows a Bode plot that consists of the magnitude of the open loop gain in dB, $A_{OL}$, and its phase in degrees.

![Circuit configuration to test for open loop gain and phase vs. frequency.](image)

Figure 2.30 shows both 1$^{st}$ dominant and 2$^{nd}$ poles occurring before the unity-gain frequency, $f_u$. This means that the output phase changes to -180° for an output gain greater than 0 dB. This op-amp is unstable. The phase
margin is $-13.6^\circ$ when the minimum practical value for stability is $45^\circ$ [Bak98].

Also gain margin is $-15.17\text{dB}$ when the minimum value required for stability is $10\ \text{dB}$ [Bak98].

Figure 2.30 $\text{A}_{\text{OL}}$ and phase for a two-Stage op-amp without compensation Capacitor.

A simulation was performed using circuit in Figure 2.26 and the following parameters: BSIM3V3 SPICE models (Appendix A), \((W/L)_{1}=207/6, (W/L)_{3,4,7}=2487/6, (W/L)_{5,6,8}=1700/6, I_{\text{SS}}=1\text{mA}, C_{L}=20\text{pF}, V_{\text{DD}}=2.5\text{V}, V_{\text{SS}}=-2.5\text{V}.$

To prevent a two-stage op-amp from becoming unstable, a compensation capacitor $C_{C}$ is used. Let’s first obtain the equations for the
dominant poles in a two-stage op-amp using the small signal models. In Figure 2.31 the parasitic capacitances that affect the dominant pole in the differential amplifier are considered.

The total capacitance at the output node of the differential amplifier is:

\[
C_{\text{tot}} = C_L + C_{db4} + C_{gd4} + C_{gb2} + C_{gd2}
\]  \hspace{1cm} (2.2.38)

Capacitance \( C_L \) in Figure 2.31 will be \( C_{gs7} \) plus \( C_{gd7}(1 + |A_v2|) \), as corroborated by Figure 2.32. \( C_{gs7} \) is multiplied by a factor \( \approx A_v2 \) because of the Miller effect [Bak98].

\[
C_{\text{tot}} = C_{gs7} + C_{gd7}*(1 + |A_v2|) + C_{db4} + C_{gd4} + C_{gb2} + C_{gd2}
\]  \hspace{1cm} (2.2.39)
From equations 2.2.25 and 2.2.39 the output node time constant is:

\[ \tau_{out1} = (r_o2||r_o4) \times C_{tot1} \]  

(2.2.40)

The pole due to this node is:

\[ f_{p1} = \frac{1}{2 \pi \tau_{out1}} \]  

(2.2.41)

The total capacitance at the output node of the second gain stage is obtained by referring to Figure 2.32:

\[ C_{tot2} = C_L + C_{db7} + C_{gd7}(1 + \frac{1}{|A_{v2}|}) + C_{gd8} + C_{gb8} + C_{gs9} + C_{gs10} \]  

(2.2.42)

Figure 2.32 Total capacitance at the output node of second gain stage.
The time constant at the drain of M7 can be calculated using equations 2.1.24 and 2.2.42:

\[ \tau_{out2} = (r_{o7} \parallel r_{o8}) \cdot C_{tot2} \]  \hspace{1cm} (2.2.43)

And a second pole is calculated similarly as equation 2.2.41:

\[ f_{p2} = \frac{1}{2 \pi \cdot \tau_{out2}} \]  \hspace{1cm} (2.2.44)

A technique known as “pole splitting” is used to compensate two-stage op-amps. This technique consists in putting a capacitor, \( C_c \), between the output of the differential pair and the output of the second gain stage. To analyze the effect of \( C_c \) on the two-stage op-amp, let’s refer to the small-signal model for a two-stage op-amp shown in Figure 2.33.

![Figure 2.33 Small-Signal Model of a Two-Stage Op-Amp in Figure 2.26.](image)

The transfer function of Figure 2.33 is:
\[
\frac{V_{\text{out}}}{V_{\text{di}}} = \frac{g_{m1}g_{m7}R_{\text{out}}^2R_{\text{out}} \left(1 - \frac{C_c}{g_{m7}}\right)}{1 + s^2 G + s^2 * H} \tag{2.2.45}
\]

\[H = C_{\text{out}}^2 + C_c * (C_{\text{out}} + C_{\text{out}}) * R_{\text{out}}^1R_{\text{out}}^2 \tag{2.2.46}\]

\[G = C_{\text{out}}^2 + C_{\text{out}}^2 * R_{\text{out}}^2 + C_c (g_{m1}R_{\text{out}}^1R_{\text{out}}^2 + R_{\text{out}}^1 + R_{\text{out}}^2) \tag{2.2.47}\]

Analyzing the denominator of equation 2.2.45, the two new poles can be found due to the introduction of capacitor \(C_c\) in the circuit:

\[fp_1 \approx \frac{1}{2 \cdot \pi \cdot \left[g_{m7} \cdot R_{\text{out}}^1 \cdot R_{\text{out}}^2 \cdot C_c \right]} \tag{2.2.48}\]

\[fp_2 \approx \frac{g_{m7} \cdot C_c}{2 \cdot \pi \cdot \left[C_{\text{out}}^2 \cdot C_{\text{out}}^2 + C_c \cdot (C_{\text{out}}^1 \cdot C_{\text{out}}^2)\right]} \tag{2.2.49}\]

From equations 2.2.48 and 2.2.49 we can see that by increasing \(C_c\), the first pole, \(fp_1\), will decrease while the second pole, \(fp_2\), will increase. Hence the name pole splitting technique.

From the gain-bandwidth relation \(ft = A_{\text{ol}} * fp_1\) and using equations 2.2.31 and 2.2.48 we can write,

\[ft = \frac{g_{m1}}{2 \cdot \pi \cdot C_c} \tag{2.2.50}\]

The transfer function in equation 2.2.47 also has a zero in:
Comparing equations 2.2.50 and 2.2.51 and noting that \( gm_1 \) and \( gm_7 \) are close in value, the zero caused by \( C_C \) is close to the unity-gain frequency, \( f_t \). This situation degrades phase margin.

To solve this problem, a resistor \( R_Z \) is added in series with capacitor \( C_C \) as seen in Figure 2.34.

When \( v_{out} = 0 \) (output zero occurring), the expression for the zero of the new transfer function is:

\[
Z = \frac{1}{2 \pi C_C \left( \frac{1}{gm_7} - R_Z \right)}
\]  
(2.2.51)

Choosing \( R_Z = \frac{1}{gm_7} \) will move the zero to infinity. For certain values of \( R_Z \), the zero may add to the phase margin, thus improving stability.

![Small-signal model with zero-canceling resistance.](image)

Figure 2.34 Small-signal model with zero-canceling resistance.
Figure 2.35 shows the Bode plot for a compensated two-stage op-amp.

The same simulation performed for Figure 2.30 was used in this plot but adding a compensation capacitor $C_c = 16\,\mu F$ and, including in series, a zero-canceling resistor $R_z = 250\,\Omega$ in the two-stage op-amp.

![Bode plot](image)

Figure 2.35 $A_{OL}$ and phase for a two-stage op-amp with compensation capacitor and zero-canceling resistor. A simulation was performed using circuit in Figure 2.26 and the following parameters: BSIM3V3 SPICE models (Appendix A), $(W/L)_1 = 207/6$, $(W/L)_{3,4,7} = 2487/6$, $(W/L)_{5,6,8} = 1700/6$, $I_{SS} = 1\,mA$, $C_L = 20\,pF$, $C_C = 16\,pF$, $R_z = 250\,\Omega$, $V_{DD} = 2.5\,V$, $V_{SS} = -2.5\,V$. 

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Figure 2.35 shows the 2\textsuperscript{nd} pole occurring after the unity-gain frequency, $f_t$. The phase margin is 60.68$^\circ$ and gain margin is 20 dB. The two-stage op-amp is stable. An interesting thing to notice about Figure 2.35 is that the 1\textsuperscript{st} and 2\textsuperscript{nd} pole are separated, in contrast to Figure 2.30 where the poles are close to each other. This proves what is suggested in equations 2.2.48 and 2.2.49, that including a compensation capacitor will decrease the frequency at which the 1\textsuperscript{st} dominant pole occur while it will increase the frequency at which the 2\textsuperscript{nd} pole occur.

In general, for 60$^\circ$ phase margin, the unity-gain frequency must be one third of the frequency were the 2\textsuperscript{nd} pole is located, [Bak98].

### 2.2.7 Two-Stage Operational Amplifier Slew Rate

The maximum voltage change with respect to time at node X in Figure 2.26 is calculated with help of slew rate equation 2.2.30:

$$\frac{dV_X}{dt} = \frac{I_{ss}}{C_{eq}} = \frac{I_{ss}}{C_C \ast (1 - Av2)} \quad (2.2.52)$$

In equation 2.2.52, $C_{eq}$ is the capacitance present at node X. This capacitance is basically the compensation capacitor times the gain of the second stage due to the Miller effect [Bak98]. We assume that parasitic capacitances of the transistors connected at node X can be neglected.
Hence, the output slew-rate of the two-stage op-amp is calculated as:

$$\frac{dV_{\text{OUT}}}{dt} = \frac{Av2 \cdot V_x}{C} = \frac{Av2 \cdot I_{\text{SS}}}{C_c \cdot (1 - Av2)} \approx \frac{I_{\text{SS}}}{C_c} \quad (2.2.53)$$

So the compensation capacitor, $C_c$, and the bias current, $I_{\text{SS}}$, determine the slew-rate of the operational amplifier.

### 2.2.8 One-Stage Operational Amplifier

One-stage op-amps, often called Operational Transconductance Amplifiers (OTA), are characterized by having all nodes at a low impedance, except for the input and output nodes. Figure 2.36 shows a typical cascode OTA. The name “cascode” is because two PMOS and two NMOS transistors, stacked one over the other, constitute the output of the OTA. This technique provides a higher output gain in comparison to using a single PMOS and NMOS transistor at the output node.

The gain of the OTA in Figure 2.36 can be calculated by finding the small signal current that flows in the differential pair:

$$i_d = \frac{gm1}{2} \cdot (V_{i2} - V_{i1}) \quad (2.2.54)$$

The current mirrors that load the differential amplifier copy this current. As a result we have two times the differential current at the output node.
The cascoded output resistance of the OTA can be estimated by looking at Figure 2.37.

\[ i_T = \frac{V_T - V_X}{\text{ro2}} + gm2 \cdot (-Vx) \]  \hspace{1cm} (2.2.55)

\[ V_X = i_T \cdot \text{ro1} \]  \hspace{1cm} (2.2.56)

![One-stage operational amplifier diagram](image)

Figure 2.36 One-stage operational amplifier.

From equations 2.2.55 and 2.2.56 we can estimate:
Figure 2.37 Small-signal model for cascode stage.

At the output node of Figure 2.36, two pairs of cascoded transistors are attached. Hence, by using equation 2.2.57, the output resistance is:

\[ \text{Rout} = \frac{V_T}{i_T} = \text{gm2} \cdot \text{ro2} \cdot \text{ro1} \quad (2.2.57) \]

To estimate the small-signal gain of the OTA shown in Figure 2.36,

\[ V_{\text{out}} = 2 \cdot K \cdot i_d \cdot \text{Rout} \quad (2.2.59) \]

And,

\[ A_{\text{OL}} = \frac{V_{\text{out}}}{V_{\text{i2}} - V_{\text{i1}}} = K \cdot \text{gm1} \cdot \text{Rout} \quad (2.2.60) \]

The constant K refers to the size relation between the input current-
mirror transistors to the output current-mirror transistors. The freedom of choosing \( K > 1 \) increases the slew-rate of the op-amp. However, increasing \( K \) will also increase power dissipation. To calculate the slew-rate for the op-amp shown in Figure 2.36 we can use equation 2.2.30 [Bak98].

The output resistance for an OTA is very high. If the OTA drives a resistive load, the load will be in parallel with the output node, thus decreasing the overall impedance and degrading the OTA gain. Therefore, OTAs cannot drive resistive loads [Bak98].

The output node of an OTA determines the dominant pole. Other nodes in the OTA will have lower impedances yielding poles at frequencies much higher than the dominant pole. By consequence, in a system that uses negative feedback, phase shifts to \( 180^\circ \) will occur at frequencies much higher than the unity-gain frequency, \( f_t \). Thus the system will always be stable without the need of compensation devices.

A disadvantage of the OTA shown in Figure 2.36 is that even though it provides a high gain, its output swing is limited because of the cascoding feature. The output of this OTA can swing from \( V_{out_{max}} = V_{DD} - 2 * V_{DSSat} \) to \( V_{out_{min}} = V_{SS} + 2 * V_{DSSat} \).

For low-voltage applications, where the total supply voltage, \( V_{DD} - V_{SS} \), is less than 1.5V, the output swing of the OTA in Figure 2.36 is prohibitively
2.2.9 Differential Pair Topologies With No Slew-Rate Limitations

The basic concept for a differential amplifier that has no slew rate limitation is shown in Figure 2.38. Under quiescent conditions, no differential signal is present, \( v_d = v_{in1} - v_{in2} = 0 \) and:

\[
V_{SG1Q} = V_{SG2Q} = V_B \quad (2.2.61)
\]

When a differential signal is present:

\[
V_{SG1} = v_d + V_B \quad (2.2.62)
\]

\[
V_{SG2} = -v_d + V_B \quad (2.2.63)
\]

Drain currents are estimated by using the square law relation under saturation condition:

\[
i_{D1} = \beta \cdot (V_{SG1} - V_{THP})^2 = \beta \cdot [v_d^2 + 2 \cdot v_d \cdot (V_B - V_{THP}) + (V_B - V_{THP})^2]
\]

\[
i_{D2} = \beta \cdot (V_{SG2} - V_{THP})^2 = \beta \cdot [(v_d^2 - 2 \cdot v_d \cdot (V_B - V_{THP}) + (V_B - V_{THP})^2]
\]

Subtracting equation 2.2.65 from equation 2.2.64 yields:

\[
i_{OUT} = i_{D1} - i_{D2} = 4 \cdot \beta \cdot v_d \cdot (V_B - V_{THP}) \quad (2.2.66)
\]
The differential output current \(i_{\text{OUT}}\) has a linear relation with the input differential voltage \(v_d\). Topologies based on the concept shown in Figure 2.38 are useful in applications where linearity between the inputs and the output differential signals is of concern. Because there is no current source in series with any of the transistors in Figure 2.38, the drain currents may increase with ideally no limitation except that of the gate-to-source voltages of transistors M1 and M2 may not exceed the power rails. Under quiescent conditions, transistors M1 and M2 are biased to a gate-to-source voltage given by equation 2.2.61. Voltage \(V_B\) may be selected to yield small drain currents equal to \(I_{\text{DQ}}\). When a large differential signal is present, one of the transistors in Figure 2.38 will be off while the other will source a large drain current. Therefore, topologies based on Figure 2.38 are known as Class-AB differential pairs.

![Figure 2.38 Conceptual circuit for Class-AB input differential pair.](image)

**2.2.9.1 Class-AB Differential Amplifier 1: Source Cross-Coupled Pair**
Figure 2.39 shows a topology to implement a NMOS version

differential pair that has no slew-rate limitations. The topology is proposed in
[Cas85] and reviewed in [Bak98]. Transistors M5 and M6 implement a floating
battery from gate of transistor M1 to gate of transistor M4. Transistors M7 and
M8 implement a floating battery from gate of transistor M2 to gate of transistor
M3. This is also shown in Figure 2.39.

![Diagram](image)

Figure 2.39 a) Source cross-coupled differential amplifier, b) Simplified schematic.

If \( V_{i1} \) increases while \( V_{i2} \) decreases, the voltage from gate to source of
transistors M1 and M3 will increase, letting \( I_{d1s} \) increase. Meanwhile, the
voltage from gate to source of transistors M2 and M4 will decrease shutting
current \( I_{d2s} \) off. The opposite will happen if \( V_{i1} \) decreases while \( V_{i2} \) increases.

Currents \( I_{d1s} \) and \( I_{d2s} \) increase with no limitation because, as seen in Figure
2.39, transistors M1 and M2 do not have a current source in series.
Let’s analyze the circuit shown in Figure 2.39 to find a relation between the input voltages to the differential currents $i_{D1s}$ and $i_{D2s}$.

$$V_{D1} = \sqrt{\frac{2 \cdot i_{D1}}{\beta_1}} + Vx + V_{THP}$$  \hspace{1cm} (2.2.67)

Current $i_{D1s}$ is estimated using the formula for drain current in saturation mode for transistor M3,

$$i_{D1s} = \frac{\beta_3}{2} \cdot (Vx + Vbias - V_{THP})^2$$  \hspace{1cm} (2.2.68)

Rearranging 2.2.67 to solve for $Vx$,

$$Vx = \sqrt{\frac{2 \cdot i_{D1}}{\beta_3}} - Vbias - V_{THP}$$  \hspace{1cm} (2.2.69)

Using equations 2.2.68 and 2.2.69 we can write an equation for $i_{D1s}$.

$$i_{D1s} = \frac{1}{2} \cdot (V_{D1} + Vbias - V_{THN} - V_{THP})^2 \cdot \frac{\beta_1 \cdot \beta_3}{\sqrt{\beta_1} + \sqrt{\beta_3}}$$  \hspace{1cm} (2.2.70)

Following a similar approach, we can write an equation for $i_{D2s}$.

$$i_{D2s} = \frac{1}{2} \cdot (V_{D2} + Vbias - V_{THN} - V_{THP})^2 \cdot \frac{\beta_2 \cdot \beta_4}{\sqrt{\beta_2} + \sqrt{\beta_4}}$$  \hspace{1cm} (2.2.71)

Figure 2.40 shows a DC transconductance characteristic plot. It includes the current waveforms, $i_{D1s}$ and $i_{D2s}$, of the source cross-coupled pair and also the current waveforms, $i_{D1}$ and $i_{D2}$, of a simple differential pairs same
as shown in Figure 2.40. As seen in the plot, the currents \( i_{D1} \) and \( i_{D2} \) corresponding to the simple differential pair have a value of \( I_{bias} = 10 \mu A \) when the input differential voltage is 0. The maximum value these currents may have is twice the bias current, \( I_{max} = I_{SS} = 20 \mu A \). On the other hand, for the source cross-coupled pair, currents \( i_{D1s} \) and \( i_{D2s} \) have a value of \( I_{bias} = 10 \mu A \) for 0 input differential voltage and may have values on the orders of 4 to 5 times the bias current.

![Graph showing DC transconductance characteristic.](image)

**Figure 2.40 DC transconductance characteristic.** A simulation was performed using circuit in Figure 2.39 and Figure 2.19, with the following parameters: BSIM3V3 SPICE models (Appendix A), a) Figure 2.39: \( (W/L)_{1,2,5,7}=17/6 \), \( (W/L)_{3,4,6,8}=51/6 \), \( I_{BIAS}=10 \mu A \), b) Figure 2.19: \( (W/L)_{1,2}=17/6 \), \( I_{SS}=20 \mu A \), Supplies: \( V_{DD}=2.5V \), \( V_{SS}=-2.5V \).

A disadvantage on topology shown in Figure 2.39 is that it requires a
minimum supply of two gate-to-source voltages plus a saturation voltage. This voltage requirement makes this topology unavailable for low-power design.

2.2.9.2 Class-AB Differential Amplifier 2: A Topology Based on the use of Flipped Voltage Follower

The differential input pair, introduced in [Pel97], is shown in Figure 2.41. Transistors M1 and M2 are the devices that handle the differential currents \(i_{D1}\) and \(i_{D2}\). Transistors M1P, M2P, M3 and M3P form two flipped-voltage followers that create a very low impedance nodes at points X and Y shown in the circuit of Figure 2.41. Having low impedance at nodes X and Y will maintain a constant gate-source voltage at transistors M1P and M2P because a constant drain current is flowing through them.

When a differential signal is input to the circuit shown in Figure 2.41, for instance, \(V_{I1}\) increases while \(V_{I2}\) decreases, the node X is pulled down while node Y is pulled up. At the same time the gate-source voltage of transistor M1 is decreased while the gate-source voltage of M2 is increased. Transistor M1 will eventually shut down while the gate-source voltage of transistor M2 may continue increasing without limitation until M3P gets out of saturation. The opposite happens when \(V_{I1}\) decreases while \(V_{I2}\) increases.

Drain currents \(i_{D1}\) and \(i_{D2}\) are governed by equations 2.2.64 and 2.2.65. Comparing Figure 2.41 to Figure 2.38, battery \(V_B\) is implemented by the gate-
to-source voltage of transistors M1P and M2P.

A nice feature of this circuit is its low voltage supply requirements.

Under static conditions,

\[ V_{supQ} = V_{DD} - V_{SS} = V_{SGQ} + V_{DSSatQ} \]  \hspace{1cm} (2.2.71)

When a differential input signal is applied, \( V_d = V_{i1} - V_{i2} \). This signal is superimposed on the quiescent gate-source voltages of transistors M1 and M2 such that, \( V_{SG1} = V_{SG1Q} - V_d \) and \( V_{SG2} = V_{SG2Q} + V_d \). Under these dynamic conditions, the supply requirements increase to:

\[ V_{sup} = V_{DD} - V_{SS} = V_{SG1Q} + V_{DSSat3} + V_d \text{ max} \]  \hspace{1cm} (2.2.72)

The drain to source voltage of M3 is given by:

\[ V_{DSSat3} = V_{DSSatQ} + V_d \text{ max} \]  \hspace{1cm} (2.2.73)

And, finally, the total dynamic supply requirement is given by:

\[ V_{sup} = V_{DD} - V_{SS} = V_{SG1Q} + V_{DSSatQ} + 2 \cdot V_d \text{ max} \]  \hspace{1cm} (2.2.74)

The very low impedance output characteristic of a flipped-voltage follower is explained by making reference to Figure 2.42. In this figure a T-model is used for the small-signal analysis [Sed98]. The following relations may be written:
\[ i_T = \frac{V_T}{r_{o3P} \left| \frac{1}{g_{m1P}} \right|} - \frac{g_{m3P} \cdot V_{SG3P} - g_{m1P} \cdot V_{SG1P}}{g_{m1P} \cdot r_{o1P} + g_{m3P}} \]  
(2.2.75)

\[ V_{SG3P} = -V_T \cdot \left(1 + g_{m1P} \cdot r_{o1P}\right) \]  
(2.2.76)

\[ V_{SG1P} = V_T \]  
(2.2.77)

Combining equations 2.2.75, 2.2.76 and 2.2.77 yields:

\[ R_{OUT} = \frac{V_T}{i_T} = \frac{1}{g_{m3P} \cdot g_{m1P} \cdot r_{o1P} + g_{m3P}} \]  
(2.2.78)

Figure 2.41 Differential pair.

The result of equation 2.2.78 shows that the output impedance of a
flipped-voltage follower is very low. Equation 2.2.78 represents the impedance found at nodes X and Y of Figure 2.41.

Figure 2.42 Flipped voltage-follower and its small-signal model.
3 A NEW CLASS-AB DIFFERENTIAL INPUT IMPLEMENTATION OF LOW-VOLTAGE HIGH SLEW RATE OP-AMPS AND LINEAR TRANSCONDUCTORS

3.1 Proposed Class-AB Differential Amplifier

The basic concept of the new Class-AB input differential pair is shown in Figure 3.1 [Ram01]. The battery is attached between the input pair transistor sources and a node that is the common-mode voltage,

\[ V_{CM} = \frac{(V_{i1} + V_{i2})}{2}, \]

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of the two input signals. The battery has a label \( V_{SGQ} \) that as will later become evident, is the source-to-gate voltage of a transistor. Node S is held at a voltage \( V_S = V_{SGQ} + V_{CM} \).

Assume a differential signal, \( v_d = v_{i1} - v_{i2} \), is present at the inputs of the amplifier. If \( v_d \) increases, the source-to-gate voltage of transistor M1 will decrease. At the same time, the source-to-gate voltage of transistor M2 will increase. Transistor M1 will eventually turn off while the gate-source voltage of transistor M2 will continue increasing with ideally no limitation. The drain currents at transistors M1 and M2 have no limitation because no current sources are in series with them.

The practical implementation of the proposed input differential amplifier is shown in Figure 3.2 [Ram01]. Similar to the topology reviewed in Section 2.2.9.2, it uses a flipped-voltage follower. The flipped-voltage follower,
constituted by transistors MCM and M3, will create very low impedance at node S, as explained in Section 2.2.9.2. Having very low impedance will maintain node S at a constant voltage \( V_S = V_{SGQ} + V_{CM} \). Again, when a differential signal is present, one of the input transistors may be driven hard with a large source-to-gate voltage in order to source a considerable amount of drain current, while the other transistor turns completely off.

![Circuit Diagram](image)

**Figure 3.1 Conceptual circuit [Ram01].**

The voltage supply requirements for the topology shown in Figure 3.2 are lower than the supply requirements for the topology proposed in Section 2.2.9.2. Under quiescent conditions, the static supply requirements for the topology in Figure 3.2 are:

\[
V_{supQ} = V_{DD} - V_{SS} = V_{SGQ} + V_{DSSat3Q} \tag{3.1.1}
\]

Equation 3.1.1 is the same as equation 2.2.71 for the topology reviewed in Section 2.2.9.2.
Figure 3.2 Input differential amplifier [Ram01].

A differential signal, \( v_d = v_{i1} - v_{i2} \), is present at the inputs of the differential amplifier. The differential input signal is superimposed over the quiescent source-to-gate voltage of transistors M1 and M2 in the following way: \( V_{SG1} = V_{SGQ} + v_d/2 \) and \( V_{SG2} = V_{SGQ} - v_d/2 \). The dynamic voltage supply requirements are then found:
\[ V_{sup} = V_{DD} - V_{SS} = V_{SGQ} + V_{DSSat3} + v_d \max /2 \]  
(3.1.2)

Since \( V_{DSSat3} = V_{DSSatQ3} + v_d \max /2 \), the final expression for dynamic voltage supply requirements is:

\[ V_{sup} = V_{DD} - V_{SS} = V_{SGQ} + V_{DSSatQ3} + v_d \max \]  
(3.1.3)

The main advantage of the topology shown in Figure 3.2 over the topology reviewed in Section 2.2.9.2 is its low dynamic voltage supply requirements, as seen by comparing equation 3.1.3 and equation 2.2.74.

The input signal-common mode voltage detector \((V_{CM})\) is shown in Figure 3.3 [Joh97].

The common mode voltage detector operates as explained below:

1. When there is no differential input signal, \( v_d = v_{i1} - v_{i2} = 0 \), each transistor in the configuration will have a drain current equal to \( I_b/2 \). The voltage at node X will be equal to the average between the two input signals,

\[ V_{CM} = \frac{(V_{i1} + V_{i2})}{2} \]  
(3.1.4)

2. When a differential input signal is present, for instance, \( V_{i1} \) increases and \( V_{i2} \) decreases by the same amount, the drain current in M1 and M3 will decrease to \( I_{D1} = I_{D3} = I_b2/2 - \Delta I \). Drain currents in M2 and M4 will increase to \( I_{D2} = I_{D4} = I_b2/2 + \Delta I \). Drain currents of transistors M2 and M3
will add at node X. Hence, the current at node X is $I_{b2}'$ and its voltage stays constant and equal to equation 3.1.4.

![Common mode voltage detector diagram](image)

Figure 3.3 Common mode voltage detector [Joh97].

(3) Suppose the input common-mode voltage increases. Drain currents in transistors M1 and M4 decrease to $I_{D1} = I_{D4} = I_{b2}'/2 - \Delta I$. Drain currents in M2 and M3 increase to $I_{D2} = I_{D3} = I_{b2}'/2 + \Delta I$. Therefore, the voltage at node X increases, keeping the relation found in equation 3.1.4. In a similar way,
when the input common-mode voltage decreases, the voltage at node \( X \) decreases but maintains the relation in equation 3.1.4.

### 3.2 Output Stage for Low-Voltage CMOS Op-Amps with Accurate Quiescent Current Control by Means of Dynamic Biasing

The basic concept behind the proposed low-voltage output stage is shown in Figure 3.4 [Car00]. It consists of two matched current sources, \( I_b' \), and a resistor. This topology allows the output stage voltage supply requirement to be kept low (\( V_{DD} - V_{SS} \geq 1.5V \)). Only a gate-to-source voltage from the output transistor plus a drain-to-source saturation voltage from the current source is needed to keep all transistors in saturation. The horizontal arrows pointing towards the ideal current sources in Figure 3.4 indicate that a quiescent current control circuit drives the ideal current sources.

The dynamic biasing for the quiescent current control is shown in Figure 3.5 (a) [Car00]. The same input control current is sunk or sourced from transistors \( M_1 \) and \( M_2 \). The source-to-gate voltage of transistor \( M_1 \) generates a voltage labeled \( V_X \) and is input to the positive terminal of a differential pair as shown. The resistor and differential amplifier that drive the current sources constitute a voltage-to-current converter. The voltage-to-current conversion is clearly seen in Figure 3.5 (b) [Car00], where the circuit is redrawn and includes practical current sources, \( M_3 \) and \( M_4 \). The voltage at node \( C \) is

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forced by feedback to be $V_X$ and consequently, $I_b' = \frac{(V_y - V_x)}{R}$. Transistors M5 to M7 form a low-voltage current mirror that helps replicate current $I_b'$ where needed.

![Diagram of low-voltage output-stage concept](image_url)

Figure 3.4 Low-voltage output-stage concept [Car00].

The complete circuit for the output stage with quiescent current control is shown in Figure 3.6 and is called "Quiescent current controlled floating battery (QCCFB)" [Car00]. The differential amplifier is implemented using PMOS transistors M10 and M11. Transistors M8/M9 and a matched resistor are used to replicate current $I_b'$ and implement a floating voltage that will drive the output transistors Moutp and Moutn.
Figure 3.5 (a) Dynamic Biasing Circuit, (b) Current-to-voltage converter [Car00].

Figure 3.6 Quiescent current controlled floating battery (QCCFB) [Car00].
3.3 Two Stage Operational Amplifier with Class-AB Input and Output Stages; the Full-AB Op-Amp

The proposed configuration is shown in Figure 3.7 and is called a Full-AB op-amp, to emphasize the use of the proposed Class-AB input and output stages. The input differential amplifier is the one reviewed in Section 3.1. The output stage used is the topology presented in Section 3.2 and, for simplicity, is shown as a resistor and two controlled ideal current sources, $I_b'$ (Figure 3.4). Components $C_C$ and $R_Z$ are used for frequency compensation, presented in Section 2.2.6. Transistors M1, M2, and M4 have their bulk terminal connected to their sources. This is done to eliminate the body effect in these transistors. Therefore, the input common-mode range is increased.

When a positive differential signal, $V_{d} = V_{i1} - V_{i2} > 0$, is present at the input of the Full-AB operational amplifier, less current will flow through transistor M2 while M1 will source more current. Therefore, the voltage at node A will decrease. Node B being a voltage $V_{AB}$ below node A, will also decrease. The source-to-gate voltage of transistor $M_{outp}$ will increase and the gate-to-source voltage of $M_{outn}$ will decrease. Hence, a large current will be delivered from the output node to an external load. The opposite happens for a negative differential voltage, $V_{d} = V_{i1} - V_{i2} < 0$. 

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Circuit QCCFB implements the floating voltage $V_{AB}$, as reviewed in Section 3.2.

3.3.1 Design Procedure for a Full-AB Op-Amp

The following specifications were considered for the design of a Full-AB op-amp as shown in Figure 3.7:

1. The full-AB op-amp will drive a 20pF load.
2. Must achieve a product Gain-Bandwidth (GBW) of 20MHz.
3. Must have a minimum slew-rate of 47 V/µs.
4. A single 1.5V voltage supply will be used.

Figure 3.7 Full-AB operational amplifier.
We can solve for the necessary transconductance of the transistors in the output stage using equation 2.2.50 in Section 2.2.6 of Chapter 2. The equation is modified for our case and rewritten below:

\[ GBW = \frac{gm_{OUT}}{2 \pi C_L} \]  \hspace{1cm} (3.3.1)

Solving for the output transconductance and using the specified load and gain-bandwidth yields:

\[ gm_{OUT} = GBW \times 2 \pi C_L = 2.513 mA/V \]  \hspace{1cm} (3.3.2)

Using the specified slew-rate and equation 2.2.30 in Section 2.2.4 of Chapter 2, we can solve for the necessary minimum output current that the output stage must be able to provide to the load.

\[ I_{total} = SR \times C_L = 942.5 \mu A \approx 1 mA \]  \hspace{1cm} (3.3.3)

For static conditions, the input and output stages will use a bias current of 100\(\mu\)A. Keeping bias currents at 1/10th the maximum required current results in less static power dissipation. Because the op-amp will be used with low-voltage supplies, the small saturation drain-to-source voltage is chosen to be \(V_{DSSat} = 0.15V\) unless otherwise specified. The Full-AB op-amp design is implemented in a CMOS 0.5-micron technology. Parameters used for the transistor design were obtained from MOSIS parametric test results for technology SCN05 AMI. The design parameters are in Table 3.1.
<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
<tr>
<td>KPN</td>
<td>Transconductance parameter NMOS</td>
<td>116μA/V²</td>
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<tr>
<td>V_{THN}</td>
<td>NMOS Threshold voltage</td>
<td>0.75V</td>
</tr>
</tbody>
</table>

Table 3.1 0.5-micron technology design parameters.

3.3.1.1 Design of the Input Stage used in the Full-AB Op-Amp

Referring to Figure 3.7, the design procedure starts with the input stage of the Full-AB operational amplifier. Transistors M1 and M2 source a bias current of $I_{D1,2} = 100\mu A$ and, with help of the saturation equation shown in (3.3.4), we can solve for dimensions W/L of the mentioned transistors. For every transistor in the design, dimension L is going to be set to 1.2μm unless otherwise specified. The design is implemented in a 0.5-micron technology such that all dimensions can be expressed in terms of a parameter $\lambda = 0.3\mu m$. For convenience, the dimensions are shown in terms of $\lambda$, i.e. $L = 4\lambda = 1.2\mu m$.

$$I_D = \frac{KP}{2} \frac{W}{L} (V_{GS} - V_{th})^2 = \frac{KP}{2} \frac{W}{L} (V_{DSSat})^2$$  \hspace{1cm} (3.3.4)
Bias current for transistor M4 in Figure 3.7 is chosen to be 4 times smaller than the bias current in transistors M1 and M2, $I_{D4} = 25\mu A$. The width for transistor M4 is:

$$ (W)_4 = \frac{(W)_{1,2}}{4} = 230\lambda = 69\mu m \quad (3.3.6) $$

As seen in Figure 3.7, the bulk connections of transistors M1, M2 and M4 are connected directly to their sources to increase the input CMR, sacrificing area.

Transistor M3 of Figure 3.7 will source a current $I_{D3} = 225\mu A$ under static conditions. A lower $V_{DSsat} = 0.14V$ is used to increase input CMR.

$$ (W)_3 = \frac{2 * I_{D3} * L}{KPP * (V_{DSsat})^2} = \frac{2 * 225\mu A * 4 * \lambda}{38.6 \frac{\mu A}{V^2} * (0.14)^2} \approx 2379\lambda = 713.8\mu m \quad (3.3.7) $$

Transistors M5 and M6 of Figure 3.7, will sink bias currents $I_{DS5,6} = 100\mu A$. Their widths are 3 times smaller than transistors M1 and M2 because NMOS transistors have a $Kpn \approx 3Kpp$ as shown in Table 3.1.

$$ (W)_{5,6} = \frac{(W)_{1,2}}{3} = 307\lambda = 92.1\mu m \quad (3.3.8) $$
The ideal current source $I_B$ in Figure 3.7 is implemented using a single current mirror formed by transistors M7 and M8. Their bias current is

$$I_{D7,8} = 25\,\mu A$$

and their dimensions are:

$$\frac{(W)}{3} = \frac{(W)_4}{3} = 75\lambda = 22.5\,\mu m$$  \hspace{1cm} (3.3.9)

Figure 3.8 shows a schematic that includes the transistor dimensions calculated above.

### 3.3.1.2 Design of the Input Common-Mode Detector

The input common-mode sensor, shown in Figure 3.3, is designed by first choosing its bias current. In our case, we choose $I_{b2'} = 10\,\mu A$.

Transistors M1 to M4 have a bias current of $I_D = 5\,\mu A$. A smaller saturation drain-to-source voltage is selected, $V_{DSsat} = 0.1\,V$, to ensure that the common-mode detector circuit will be on for any suitable input signal applied to the input differential amplifier in the Full-AB op-amp. Dimension L is set to $4\lambda$ or $1.2\,\mu m$ unless otherwise specified.

Using equation 3.3.4 the dimensions for transistors M1 to M4, in Figure 3.3, are obtained:
\[(W)_{1-4} = \frac{2 \cdot I_D \cdot L}{KPP \cdot (V_{DSSat})^2} = \frac{2 \cdot 5\mu A \cdot 4\lambda}{38.6 \mu A \cdot (0.1)^2} \approx 103\lambda = 30.9\mu m \quad (3.3.10)\]

\[(W)_{5-7} = (W)_{1-4} \cdot 2 \approx 207\lambda = 62.1\mu m \quad (3.3.11)\]

Transistors M5 to M7 are PMOS current mirrors used to generate \(Ib2' = 10\mu A\) in Figure 3.3, hence, their widths are:

Transistors M8 to M10 are NMOS current mirrors used to sink
$Ib2' = 10\mu A$ in Figure 3.3 and their widths are designed for

$$V_{DSat8-10} = 0.08V :$$

$$\left(W\right)_{8-10} = \frac{2 * I_{b2''} L}{K_{Pn} * (V_{DSat8-10})^2} \approx 108\lambda = 32.4\mu m \quad (3.3.12)$$

Figure 3.9 shows a complete schematic for the input common-mode detector, including transistor sizes designed above.

### 3.3.1.3 Design for Class-AB Output Stage and QCCFB Circuit

Referring to Figure 3.7, the design of the output stage transistors $M_{outp}$ and $M_{outn}$ is as follows. The maximum current that the output stage will be able to deliver to an external load is chosen to be 3mA. Maximum delivered current to a load will occur when a minimum voltage at the gate terminal of the output PMOS transistor will be 0.15V above $V_{SS}$. Using the saturation equation, the width for output PMOS transistor is calculated. The length is chosen to be $L_N = 2\lambda = 0.6\mu m$.

$$\left(W\right)_{OUTP} = \frac{2 * I_{DOUTMAX} * L_p}{K_{Pp} * (V_{SGP} - V_{thp})^2} = \frac{2 * 3mA * 2\lambda}{38.6 \mu A * V^2 * (1.35 - 0.9)^2} \approx 1535\lambda = 460.5\mu m \quad (3.3.13)$$
Figure 3.9 Input common-mode detector with transistor sizes.

The sizing of the Moutn transistor, in Figure 3.7, is simply three times smaller than the PMOS output transistor, because NMOS transistors have a $K_{Pn} \approx 3K_{Pp}$ as seen in Table 3.1:

$$\frac{(W)_{OUTN}}{3} = \frac{(W)_{OUTP}}{3} \approx 510 \lambda = 153 \mu m$$ (3.3.14)

The floating voltage $V_{AB}$ in Figure 3.7 is implemented with the circuit reviewed in Section 3.2 and shown in Figure 3.6. Transistors M1 and M2 in
Figure 3.6 are replicas of output transistors Moutn and Moutp scaled down by a factor of 10. The current sunk and sourced from transistors M1 and M2 is \( I_1 = 10 \mu A \). As such, the gate-to-source voltages generated in the diode-connected transistors M1 and M2 will be the same as the gate-to-source voltages generated in the output transistors Moutn and Moutp, respectively. Hence, having a current \( I_1 = 10 \mu A \) will cause the bias output current to be \( I_{OUT} = 100 \mu A \).

\[
(W)_1 = \frac{(W)_{OUTN}}{10} = 51\lambda = 15.3 \mu m \quad \text{and} \quad (L)_1 = 2\lambda = 0.6 \mu m \quad (3.3.15)
\]

\[
(W)_2 = \frac{(W)_{OUTP}}{10} = 153\lambda = 45.9 \mu m \quad \text{and} \quad (L)_2 = 2\lambda = 0.6 \mu m \quad (3.3.16)
\]

The two current sources with \( I_1 = 10 \mu A \) of Figure 3.6 are generated with a current mirror circuit like the one shown in Figure 3.10. This section of the output stage includes the diode-connected transistors M1 and M2 designed above. Widths for the NMOS transistors in the current mirror are designed first, with \( L = 4\lambda = 1.2 \mu m \) and \( V_{DSsat} = 0.15V \):

\[
(W)_{ib-4b} = \frac{2 \cdot I_1 \cdot L}{K_{Pn} \cdot (V_{DSsat})^2} = \frac{2 \cdot 10 \mu A \cdot 4\lambda}{116 \frac{\mu A}{V^2} \cdot (0.15)^2} \approx 31\lambda = 9.3 \mu m \quad (3.3.17)
\]

Widths for the current mirror PMOS transistors in Figure 3.10, with \( L = 4\lambda = 1.2 \mu m \) and \( V_{DSsat} = 0.15V \), are:
\[ (W)_{5b-7b} = (W)_{1b-4b} \times 3 \approx 93 \lambda = 27.9 \mu m \] (3.3.18)

Biasing voltages \( V_{BIASP} = 0.2V \) and \( V_{BIASN} = 1.2V \) are selected to keep the cascoded transistors in saturation.

Next, the design for the differential amplifier used in Figure 3.6 is presented. Transistors M10 and M11 in Figure 3.6 are designed to source a current \( I_{D10-11} = 5 \mu A \). Using \( V_{DSsat10-11} = 0.05V \) and \( L = 6 \lambda = 1.8 \mu m \). The widths of these transistors are:

Figure 3.10 Input transistors M1 and M2 of the quiescent current controlled output stage and including current mirror to generate current I1.
\[
(W)_{10-11} = \frac{2 \cdot I_{D10-11} \cdot L}{KPp \cdot (V_{DSSat10-11})^2} = \frac{2 \cdot 5 \mu A \cdot 6 \lambda}{38.6 \frac{\mu A}{V^2} \cdot (0.05)^2} \approx 622 \lambda = 186.6 \mu m
\]

(3.3.19)

The widths of transistors M10 and M11 were doubled in simulation to allow for higher input common-mode range and use of \( I_1 < 10 \mu A \):

\[
(W)_{10-11} = 1244 \lambda = 373.3 \mu m
\]

(3.3.20)

The differential amplifier used in Figure 3.6 is shown again in Figure 3.11 but includes current mirrors that implement the 10\( \mu A \) and 5\( \mu A \) current sources. Transistor M5da is designed for \( V_{DSSat5da} = 0.05 V \), \( I_{D5da} = 10 \mu A \) and \( L = 6 \lambda = 1.8 \mu m \).

\[
(W)_{10-11} = \frac{2 \cdot I_{D5da} \cdot L}{KPp \cdot (V_{DSSat5da})^2} = \frac{2 \cdot 10 \mu A \cdot 6 \lambda}{38.6 \frac{\mu A}{V^2} \cdot (0.05)^2} \approx 1244 \lambda = 373.3 \mu m
\]

(3.3.21)

The width of transistor M5da, in Figure 3.11, was modified in simulation to allow for higher common-mode input range and the use of \( I_1 < 10 \mu A \):

\[
(W)_{5da} = 1500 \lambda = 450 \mu m
\]

(3.3.22)
Transistor M4da, in Figure 3.11, sources 5µA so its width is half the width of transistor M5da:

\[(W)_{4da} = 750\lambda = 225\mu m\]  
(3.3.23)

NMOS transistors M1da to M3da, in Figure 3.11, sink a 5µA current. These transistors are designed for \(V_{DSsat}^{1da} = 0.1 V\), \(I_{D1da} = 5 \mu A\) and \(L = 6\lambda = 1.8 \mu m\).

\[(W)_{1da-3da} = \frac{2 * I_{D1da} * L}{Kp n * (V_{DSsat}^{1da})^2} = \frac{2 * 5 \mu A * 6\lambda}{116 \mu A V^2 * (0.1)^2} \approx 52\lambda = 15.6 \mu m\]  
(3.3.24)

Finally, to complete the output stage with quiescent current control, the design for the circuit that will generate the floating voltage \(V_{AB}\) is presented below.

Referring to Figure 3.6, the widths for transistors M3 to M9 are first determined. All transistors are designed for \(V_{DSsat} = 0.11 V\), \(I_D = 10 \mu A\) and \(L = 6\lambda = 1.8 \mu m\).

Starting with NMOS transistors M4, M6, M7 and M9 of Figure 3.6, their widths are calculated below:

\[(W)_{4,6,7,9} = \frac{2 * I_D * L}{Kp n * (V_{DSsat})^2} = \frac{2 * 10 \mu A * 6\lambda}{116 \mu A V^2 * (0.11)^2} \approx 83\lambda = 24.9 \mu m\]  
(3.3.25)
Figure 3.11 The differential amplifier used in Figure 3.6, including current mirrors to generate 10\(\mu\)A and 5\(\mu\)A current sources.

The PMOS transistors M3, M5 and M8 of Figure 3.6, have widths 3 times larger than the NMOS transistors:

\[
(W)_{3,5,8} = (W)_{4,6,7,9} \times 3 = 249\lambda = \text{74.7\(\mu\)m} \quad (3.3.26)
\]

Referring to Figure 3.6, the voltage across resistor R is

\[V_{AB} = V_y - V_x' \approx 0.3V\]

and the resistor value is chosen to be \(R = 30k\Omega\) for a 10\(\mu\)A current.
A schematic that includes all transistor dimensions in this last stage of design is shown in Figure 3.12.

![Figure 3.12 Output transistors with quiescent current controlled floating voltage circuit.](image)

A DC voltage \( V_{BIASN2} = 1.4V \) is applied to the gate of transistor M6 and that leaves 0.4 volts for the drain-to-source voltage of transistor M7.

### 3.3.2 Analysis of the Designed Full-AB Op-Amp

In this section the Full-AB operational amplifier designed in Section 3.3.1 is analyzed. A theoretical analysis is done to estimate the Op-amp gain,
unity-gain frequency and power consumption. Simulations, with BSIM3V3 SPICE models, are performed to calculate the parameters mentioned above. The BSIM3V3 SPICE models, used in simulations throughout this text, are provided in Appendix A. Finally a comparison between theoretical estimated and simulated parameters is provided.

### 3.3.2.1 Input Voltage Common-Mode Range

Similar to the procedure reviewed in Section 2.2.2, we obtain the maximum and minimum common-mode voltages that can be present at the inputs of the differential amplifier shown in Figure 3.8:

\[
Vin_{Q,\text{MAX}} = V_{DD} - V_{DSs1} - V_{SS} = 0.3V \quad (3.3.27)
\]

\[
Vin_{Q,\text{MIN}} = V_{SS} + V_{GS5} + V_{DSs1} - V_{SS} = 0 \quad (3.3.28)
\]

The common-mode input range for the operational amplifier is located close to the negative voltage rail, $V_{SS}$. It is typical for low-voltage op-amp design that both terminals operate close to one of the supply rails [Ram00]. For biasing purposes, the common-mode input voltage is chosen to be $Vin_Q = 0.15V$, that is, in the middle of the range delimited by results in equations 3.3.27 and 3.3.28.
3.3.2.2 Theoretical Estimation of Gain, Static Power Dissipation and Unity-Gain Frequency for the Designed Full-AB Op-Amp

3.3.2.2.1 Full-AB Op-Amp Gain

In Figure 3.7, nodes A and Vout are high impedance nodes where the gain of the overall amplifier is determined. With the help of equations 2.2.23 and 2.2.25 from Chapter 2, the impedance at node A due to transistors M2 and M6 in the op-amp shown in Figure 3.7 is calculated.

\[
ro2 = ro6 = \frac{1}{\lambda o * I_D} = \frac{1}{0.1V^{-1} \times 100\mu A} = 100k\Omega
\]

(3.3.29)

\[
R_A' = ro2 \parallel ro6 = 50k\Omega
\]

(3.3.30)

The value for channel length modulation, \(\lambda o = 0.1V^{-1}\), is estimated from simulations of MOS transistors with length \(L = 1.2\mu m\). The floating battery attached to node A in Figure 3.7 contributes to its impedance. Referring to Figure 3.6 and Figure 3.13, a section of the QCCFB circuit attached to node A is analyzed with the small signal model.
Figure 3.13 Small signal model for the section of QCCFB attached to node A.

The contribution to impedance in node A due to the QCCFB circuit is estimated by:

\[ L = 1.8\mu m, \quad \lambda_{OFB} = 0.05 V^{-1} \text{ and } I_{DFB} = 10 \mu A \quad (3.3.31) \]

\[ ron = rop = \frac{1}{\lambda_{OFB} I_{DFB}} = \frac{1}{0.05 V^{-1} \times 10 \mu A} = 2 M\Omega \quad (3.3.32) \]

\[ R_{FB} = rop \| ron + 30k\Omega \approx 1 M\Omega \quad (3.3.33) \]

The total impedance at node A is:

\[ R_A = R_A \| R_{FB} = 47.62k\Omega \quad (3.3.34) \]
The transconductance of transistor M1 in Figure 3.7 is:

\[ gm_1 = \sqrt{2I_D \cdot KPP \cdot (W)}_{L} = \sqrt{2 \cdot 100 \mu A \cdot 38.6 \frac{\mu A}{V^2} \cdot \frac{921}{4}} = 1.333 \frac{mA}{V} \]  

(3.3.35)

Using equation 2.2.27 in Chapter 2, the gain of the first stage in the circuit shown in Figure 3.7 is calculated.

\[ A_1 = gm_1 \cdot R_A = 63.48 \frac{V}{V} \]  

(3.3.36)

In a similar way, the gain of the output stage is calculated. First the impedance at node Vout is estimated:

\[ L = 0.6 \mu m, \quad \lambda_{out} = 0.15 V^{-1} \quad \text{and} \quad I_{D_{out}} = 100 \mu A \]  

(3.3.37)

\[ r_{o_{outn}} = r_{o_{outp}} = \frac{1}{\lambda_{o_{out}} \cdot I_{D_{out}}} = \frac{1}{0.15 V^{-1} \cdot 100 \mu A} = 66.67 k\Omega \]  

(3.3.38)

\[ R_{out} = r_{o_{outn}} || r_{o_{outp}} = 33.33 k\Omega \]  

(3.3.39)

The gain of the output stage is calculated with the help of equation 2.1.23 in chapter 2.

\[ gm_{outp} = \sqrt{2I_{D_{outp}} \cdot KPP \cdot (W)_{outp}}/L = \sqrt{2 \cdot 100 \mu A \cdot 38.6 \frac{\mu A}{V^2} \cdot \frac{1535}{2}} = 2.43 \frac{mA}{V} \]  

(3.3.40)

\[ gm_{outn} = gm_{outp} \]  

(3.3.41)
\[ A_{OUT} = -(gm_{OUTP} + gm_{OUTN}) \cdot R_{OUT} = -162.3 \text{V/V} \quad (3.3.42) \]

The overall gain is estimated to be:

\[ A_{OL} = A_i \cdot A_{OUT} = -10300 \text{V/V} \quad (3.3.43) \]

\[ |A_{OL}| dB = 80.2 dB \quad (3.3.44) \]

3.3.2.2.2 Full-AB Op-Amp Static Power Estimation

To calculate the total static power dissipation in the designed Full-AB amplifier we first calculate the total current provided by voltage supply \( V_{DD} \).

The total current supplied by \( V_{DD} \) in the input stage of the op-amp is shown in Figure 3.8.

\[ I_{INPUT} = 250 \mu A \quad (3.3.45) \]

The total current supplied by \( V_{DD} \) in the input common-mode detector of the op-amp is shown in Figure 3.9.

\[ I_{VCM} = 40 \mu A \quad (3.3.46) \]

The total current supplied by \( V_{DD} \) in the quiescent current controlled output stage of the op-amp is shown in Figures 3.10, 3.11 and 3.12.

\[ I_{OUTPUT} = 190 \mu A \quad (3.3.47) \]

Therefore, the total current supplied by \( V_{DD} \) and the total static power
dissipated in the Full-AB op-amp are calculated:

\[ I_{TOTAL} = I_{INPUT} + I_{VCM} + I_{OUTPUT} = 480 \mu A \]  
(3.3.48)

\[ P_{STATIC} = I_{TOTAL} \cdot V_{DD} = 720 \mu W \]  
(3.3.49)

### 3.3.2.3 Full-AB Op-Amp Simulation Results

The designed Full-AB op-amp was simulated to verify performance characteristics such as gain, static power dissipation, unity-gain frequency, systematic offset, maximum output swing and slew-rate. Simulations were done using SPICE BSIM3V3 models from a 0.5-micron N-well CMOS technology. The SPICE simulation file for the Full-AB op-amp is provided in Appendix A.

#### 3.3.2.3.1 Output Voltage Transfer Characteristic Curve

The first simulation performed using the designed Full-AB op-amp consists of a DC sweep of the positive input terminal while holding the negative input terminal to a known DC value and monitoring the voltage at the output node. The test setup is shown in Figure 3.14 and the simulated output voltage is shown in Figure 3.15.
Figure 3.14 DC Sweep test setup for output voltage transfer characteristic curve measurement.

Figure 3.15 Output voltage transfer characteristic curve.
The following parameters were measured using the result shown in Figure 3.15.

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input offset voltage</td>
<td>3.18mV</td>
</tr>
<tr>
<td>Open-loop gain, Aol (V/V)</td>
<td>2821V/V</td>
</tr>
<tr>
<td>Open-loop gain, Aol (dB)</td>
<td>69 dB</td>
</tr>
<tr>
<td>Output voltage swing</td>
<td>1.24V</td>
</tr>
<tr>
<td>Static Power</td>
<td>700.3µW</td>
</tr>
</tbody>
</table>

Table 3.2 DC sweep simulation results.

Since a single voltage supply, $V_{DD}$, is being used to feed the op-amp, all input and output signals will be in the range of 0 and 1.5V. The input offset voltage was calculated by determining the necessary input voltage to generate an output voltage equal to 0.75V, which is the middle point of the supply rails. Static power dissipation is calculated by monitoring the total output current supplied by $V_{DD}$ when the output voltage is equal to 0.75V. Gain is calculated by obtaining the slope of the output curve where it is linear and the output swing is the range where the output increases linearly.
3.3.2.3.2 Output Current Transfer Characteristic

A DC sweep analysis was performed to verify the Class-AB operation at the output stage. The simulation was performed using the test setup shown in Figure 3.16. The 0.75V source used in Figure 3.16 is used to maintain both output transistors in saturation.

![Figure 3.16 DC sweep test setup for current transfer characteristic curve measurement.](image)

The DC output current transfer curve is shown in Figure 3.17. The quiescent output current is 0.112mA but for a large differential signal, currents greater than 1mA can be delivered to an external load.
3.3.2.3.3 Verification of Quiescent Current Control Circuit

Figure 3.18 shows the output bias current vs. input control current, Iq. The plot shows that for increasing input current control, the output bias current increases. In other words, the floating battery, $V_{AB}$, increases as the input control current increases.
Figure 3.18 Output bias current vs. input control current, Iq.

### 3.3.2.3.4 Frequency Domain Analysis

The following is an AC sweep and it was performed in order to test the open-loop gain of the Full-AB op-amp. The AC sweep simulation is useful to measure the amplifier gain, unity-gain frequency and stability. The test setup is shown in Figure 3.19 and reviewed in Section 2.2.6 of Chapter 2. A new feature in Figure 3.19, which is not discussed in Chapter 2, is the 0.6V floating battery attached between the output and the negative input [Ram98]. This floating battery is needed for low-voltage applications in order to set the...
common-mode input range of the amplifier close to one of the supply rails. In the case of Figure 3.19, the feedback loop applied to the amplifier will hold the negative input to 0.15V. Using a floating voltage value at 0.6V will keep the output node at 0.75V. If we make reference to Figure 3.15, it is seen that the output voltage equal to 0.75V is the middle point where the voltage is linear. If the floating voltage 0.6V were not used, the output voltage would be 0.15V and referencing to Figure 3.15; the output is located in a non-linear region where the open loop gain is degraded.

![Figure 3.19 AC sweep test setup.](image)

A Bode plot obtained from the AC sweep analysis is shown in Figure 3.20 and the simulation results are shown in Table 3.3.
<table>
<thead>
<tr>
<th>Measurement</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Margin</td>
<td>58.85°</td>
</tr>
<tr>
<td>Gain Margin</td>
<td>18.42 dB</td>
</tr>
<tr>
<td>Unity-gain frequency (ft)</td>
<td>35.54MHz</td>
</tr>
<tr>
<td>Open loop gain (Aol)</td>
<td>2879V/V</td>
</tr>
<tr>
<td>Aol dB</td>
<td>69.18 dB</td>
</tr>
</tbody>
</table>

Table 3.3 AC sweep analysis results.

The AC sweep analysis helps determine the required capacitor and resistor values for the stability compensation circuit connected between node A and Out in Figure 3.7. It is difficult to estimate these values theoretically. Frequency compensation is described in detail in Section 2.2.6 in Chapter 2. To compensate the designed Full-AB op-amp, the following procedure was used. First, resistor Rz is theoretically estimated using the result in equation 2.2.51, but given that a Class AB output was used instead of a Class A for which equation 2.2.51 was developed, a modification is made:

$$R_z = \frac{1}{gm_{OUTP} + gm_{OUTN}} = \frac{1}{4mA/v} = 250\Omega$$  \hspace{1cm} (3.3.50)
For capacitor $C_c$, the estimation is done differently. The output stage must be able to provide 1mA to a 20pF load. The input stage has a bias current that is $1/10^{th}$ the maximum output current. Therefore capacitor $C_c$ is chosen as $1/10^{th}$ the output load.

$$C_c = 2\, pF$$  \hfill (3.3.51)

The AC sweep analysis simulations were initially performed with the estimated values of $R_z$ and $C_c$. These values were modified in the simulation to obtain optimum stability results, $PM=60^\circ$ [Bak98]. An extra compensation...
capacitor, $C_{c2}$, was added between nodes A and B to further improve the stability performance of the Full-AB op-amp. The final values for the frequency-compensation circuit are shown in Table 3.4.

<table>
<thead>
<tr>
<th>Compensation Element</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{c}$</td>
<td>4.4pF</td>
</tr>
<tr>
<td>$R_z$</td>
<td>1.5kOhm</td>
</tr>
<tr>
<td>$C_{c2}$</td>
<td>2pF</td>
</tr>
</tbody>
</table>

Table 3.4 Frequency compensation circuit elements.

**3.3.2.3.5 Transient Analysis**

To calculate the slew-rate for the Full-AB amplifier, a transient analysis is performed. The test setup used for the transient analysis is a voltage inverter and it is shown in Figure 3.21. Similar to Figure 3.19, the test setup shown in Figure 3.21 includes a 0.6V floating battery between the feedback network and the negative terminal. A single voltage follower configuration, like the one shown in Chapter 2, Section 2.2.6, is not suitable to calculate slew-rate for the designed Full-AB op-amp because the inputs to the amplifier must be kept low and close to the negative rail in order to have all the transistors in saturation with low supply voltages. Having small input signals to the voltage follower configuration will generate small changes in the source-to-gate voltages of the input pair and thus not push the device to source or sink large
currents to an external load. The inverter amplifier shown in Figure 3.21 will maintain both inputs of the Full-AB amplifier to 0.15V and only when the input signal changes abruptly is when the input terminals of the Full-AB op-amp will sense a differential signal. Hence the inverter amplifier can be tested with a rail-to-rail (0-1.5V) squared input signal that creates a maximum differential voltage of 0.75V between the input terminals of the op-amp. Thus, the Full-AB op-amp will be forced to source or sink the maximum output current.

Figure 3.21 Voltage inverter test setup.

Figure 3.22 shows simulated transient analysis plots for the input-output voltage signals and the currents in the compensation and load capacitance of the voltage inverter. The input signal used to test the circuit is a square wave signal, rail-to-rail (0-1.5V) at 5MHz. The slewing effect is
evident in the voltage plots. It is seen that the output stage sources or sinks more than 1mA to the output load.

Figure 3.22 Transient analysis plots.

The calculated slew rate for the output signal going down and up is shown in Table 3.5.

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR rise</td>
<td>53.16V/µs</td>
</tr>
<tr>
<td>SR fall</td>
<td>52.22V/µs</td>
</tr>
</tbody>
</table>

Table 3.5 Transient analysis results.
3.3.2.3.6 Theoretical vs. Simulated Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Theoretical result</th>
<th>Simulated result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aol dB</td>
<td>80.2 dB</td>
<td>69 dB</td>
</tr>
<tr>
<td>Static power</td>
<td>720µW</td>
<td>700.3µW</td>
</tr>
<tr>
<td>Unity-gain frequency (ft)</td>
<td>48.22MHz</td>
<td>35.54MHz</td>
</tr>
<tr>
<td>SR</td>
<td>47V/µs</td>
<td>52.23V/µs</td>
</tr>
</tbody>
</table>

Table 3.6 Theoretical vs. Simulated results.

There are some differences between theoretical estimated results and simulated results. The theoretical gain is higher than simulated gain by 10 dB that is 5 times higher than the simulated open-loop gain. This difference may be because the transistor’s channel length modulation value, $\lambda o$, used in the gain estimation is not accurate. For the input stage I used $\lambda o_{2,6} = 0.1V^{-1}$ for transistors M2 and M6 that have an $L = 1.2\mu m$. Circuit QCCFB contributes to the node resistance that determines the gain of the input stage. I assumed a $\lambda o_{FB} = 0.05V^{-1}$ for the QCCFB transistors involved in the gain estimation, M8 and M9 with $L = 1.8\mu m$. Finally, I assumed a $\lambda o_{OUT,N,P} = 0.15V^{-1}$ for the output transistors in the second stage, which have a $L = 0.6\mu m$.

I also tried estimating the channel length modulation of each transistor by simulating their $I_D$ vs. $V_{DS}$ characteristic curve and estimating $\lambda o$ from the
resulting plot. The resulting $\lambda_0$s are $\lambda_0 = 0.0451 V^{-1}$, $\lambda_0 = 0.0308 V^{-1}$, $\lambda_0 = 0.0223 V^{-1}$, $\lambda_0 = 0.0285 V^{-1}$, $\lambda_{OUTP} = 0.109 V^{-1}$ and $\lambda_{OUTN} = 0.0524 V^{-1}$. Calculating the open-loop gain with these channel length modulation values result in a gain of 93.4 dB.

Unity-gain frequency, $f_t$, estimated result is higher than the simulated result. Using equation 2.2.50 and showed again in equation 3.3.52, we can estimate a unity-gain frequency:

$$f_t = \frac{g_{m1,2}}{2 * \pi * C_c} = \frac{1.333 mA/\nu}{2 * \pi * 4.4 pF} = 48.22 MHz$$  \hspace{1cm} (3.3.52)

Equation 3.3.52 is derived from the op-amp’s open-loop gain equation and it neglects contributions to the gain due to the transistor resistances and parasitic capacitances in the nodes that determine the op-amp’s gain. Taking these gain contributions into account with equation 3.3.52 may give a result that is closer to the simulated unity-gain frequency result. Full-AB op-amp design has a performance that exceeds the initial design specifications. Unity-gain frequency, $f_t$, obtained in simulation is higher than 20MHz as initially specified. Initial slew-rate specification is 47V/$\mu$s while Full-AB simulated slew-rate is 52.23 V/$\mu$s.
3.3.2.4 Topology Comparison

This section shows a comparison between the designed Full AB against a Full-A (Class-A input, Class-A output) topology and a Class A-AB (Class-A input, Class-AB output) topology. The Class A-AB topology uses the same output stage as the Full-AB topology. SPICE simulation files for Full-A and Class A-AB op-amps are provided in Appendix A.

The schematic for the Full-A topology is shown in Figure 3.23. Table 3.7 contains the capacitor and resistor values for Full-A frequency compensation circuit. The transistor sizes are specified in Table 3.8. Table 3.9 specifies Full-A bias currents.

![Figure 3.23 Class-A input, Class-A output (Full-A).](image)

Figure 3.23 Class-A input, Class-A output (Full-A).
<table>
<thead>
<tr>
<th>Device</th>
<th>Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cc</td>
<td>Capacitor</td>
<td>4pF</td>
</tr>
<tr>
<td>Rz</td>
<td>Resistor</td>
<td>1.5kOhms</td>
</tr>
</tbody>
</table>

Table 3.7 Full-A compensation circuit.

<table>
<thead>
<tr>
<th>Device</th>
<th>Type</th>
<th>Width (λ)</th>
<th>Width (μm)</th>
<th>Length (λ)</th>
<th>Length (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>PMOS</td>
<td>921λ</td>
<td>276.3μm</td>
<td>4λ</td>
<td>1.2μm</td>
</tr>
<tr>
<td>M2</td>
<td>PMOS</td>
<td>921λ</td>
<td>276.3μm</td>
<td>4λ</td>
<td>1.2μm</td>
</tr>
<tr>
<td>M3</td>
<td>PMOS</td>
<td>1842λ</td>
<td>552.6μm</td>
<td>4λ</td>
<td>1.2μm</td>
</tr>
<tr>
<td>M3</td>
<td>PMOS</td>
<td>921λ</td>
<td>276.3μm</td>
<td>4λ</td>
<td>1.2μm</td>
</tr>
<tr>
<td>M4</td>
<td>PMOS</td>
<td>921λ</td>
<td>276.3μm</td>
<td>4λ</td>
<td>1.2μm</td>
</tr>
<tr>
<td>M5</td>
<td>NMOS</td>
<td>307λ</td>
<td>92.1μm</td>
<td>4λ</td>
<td>1.2μm</td>
</tr>
<tr>
<td>M6</td>
<td>NMOS</td>
<td>307λ</td>
<td>92.1μm</td>
<td>4λ</td>
<td>1.2μm</td>
</tr>
<tr>
<td>Moutp</td>
<td>PMOS</td>
<td>1842λ</td>
<td>552.6μm</td>
<td>4λ</td>
<td>1.2μm</td>
</tr>
<tr>
<td>Moutn</td>
<td>NMOS</td>
<td>307λ</td>
<td>92.1μm</td>
<td>2λ</td>
<td>0.6μm</td>
</tr>
</tbody>
</table>

Table 3.8 Full-A device sizing.
Table 3.9 Full-A bias currents.

<table>
<thead>
<tr>
<th>Biasing label</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_B$</td>
<td>100,\mu\text{A}</td>
</tr>
<tr>
<td>$I_{B\text{OUT}}$</td>
<td>1000,\mu\text{A}</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>1.5,V</td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>0,V</td>
</tr>
</tbody>
</table>

The Class A-AB topology is shown in Figure 3.24. Class A-AB uses the same QCCFB circuit as Full-AB op-amp. Table 3.10 contains the capacitor and resistor values for Class A-AB frequency compensation circuit. Table 3.11 specifies Class A-AB bias currents. Transistor sizes are specified in Table 3.12.

Table 3.10 Class A-AB compensation circuit.

<table>
<thead>
<tr>
<th>Device</th>
<th>Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cc</td>
<td>Capacitor</td>
<td>4.4,pF</td>
</tr>
<tr>
<td>Rz</td>
<td>Resistor</td>
<td>2,pF</td>
</tr>
<tr>
<td>Cc2</td>
<td>Capacitor</td>
<td>1.5k,\text{Ohms}</td>
</tr>
</tbody>
</table>

Table 3.11 Class A-AB bias currents.
Figure 3.24 Class-A input, Class-AB output (Class A-AB).

<table>
<thead>
<tr>
<th>Biasing label</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_B$</td>
<td>100$\mu$A</td>
</tr>
<tr>
<td>$I_{BOUT}$</td>
<td>100$\mu$A</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>1.5V</td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>0V</td>
</tr>
</tbody>
</table>

Table 3.11 Class A-AB bias currents.
<table>
<thead>
<tr>
<th>Device</th>
<th>Type</th>
<th>Width ($\lambda$)</th>
<th>Width ($\mu$m)</th>
<th>Length ($\lambda$)</th>
<th>Length ($\mu$m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>PMOS</td>
<td>921$\lambda$</td>
<td>276.3$\mu$m</td>
<td>4$\lambda$</td>
<td>1.2$\mu$m</td>
</tr>
<tr>
<td>M2</td>
<td>PMOS</td>
<td>921$\lambda$</td>
<td>276.3$\mu$m</td>
<td>4$\lambda$</td>
<td>1.2$\mu$m</td>
</tr>
<tr>
<td>M3</td>
<td>PMOS</td>
<td>1842$\lambda$</td>
<td>552.6$\mu$m</td>
<td>4$\lambda$</td>
<td>1.2$\mu$m</td>
</tr>
<tr>
<td>M4</td>
<td>PMOS</td>
<td>921$\lambda$</td>
<td>276.3$\mu$m</td>
<td>4$\lambda$</td>
<td>1.2$\mu$m</td>
</tr>
<tr>
<td>M5</td>
<td>PMOS</td>
<td>307$\lambda$</td>
<td>92.1$\mu$m</td>
<td>4$\lambda$</td>
<td>1.2$\mu$m</td>
</tr>
<tr>
<td>M6</td>
<td>PMOS</td>
<td>307$\lambda$</td>
<td>92.1$\mu$m</td>
<td>4$\lambda$</td>
<td>1.2$\mu$m</td>
</tr>
<tr>
<td>M7</td>
<td>PMOS</td>
<td>300$\lambda$</td>
<td>90$\mu$m</td>
<td>4$\lambda$</td>
<td>1.2$\mu$m</td>
</tr>
<tr>
<td>M8</td>
<td>PMOS</td>
<td>75$\lambda$</td>
<td>22.5$\mu$m</td>
<td>4$\lambda$</td>
<td>1.2$\mu$m</td>
</tr>
<tr>
<td>Moutp</td>
<td>PMOS</td>
<td>1535$\lambda$</td>
<td>460.5$\mu$m</td>
<td>2$\lambda$</td>
<td>0.6$\mu$m</td>
</tr>
<tr>
<td>Moutn</td>
<td>NMOS</td>
<td>510$\lambda$</td>
<td>153$\mu$m</td>
<td>2$\lambda$</td>
<td>0.6$\mu$m</td>
</tr>
<tr>
<td>QCCFB</td>
<td>Floating Battery</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3.12 Class A-AB device sizing.
A performance comparison is shown in Table 3.13 and Table 3.14. The results of these tables were obtained by performing DC, AC and transient simulations.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Aol (dB)</th>
<th>Static Power (µW)</th>
<th>Input offset voltage (mV)</th>
<th>Output voltage swing (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-A</td>
<td>65.8 dB</td>
<td>717.7 µW</td>
<td>1.68 mV</td>
<td>1.16 V</td>
</tr>
<tr>
<td>Class A-AB</td>
<td>69.06 dB</td>
<td>778.4 µW</td>
<td>3.21 mV</td>
<td>1.24 V</td>
</tr>
<tr>
<td>Full-AB</td>
<td>69 dB</td>
<td>700.3 µW</td>
<td>3.18 mV</td>
<td>1.24 V</td>
</tr>
</tbody>
</table>

Table 3.13 Topology performance comparison table.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Phase Margin (°)</th>
<th>Gain Margin (dB)</th>
<th>Unity-gain frequency (MHz)</th>
<th>Slew-rate (V/µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-A</td>
<td>59.55°</td>
<td>23 dB</td>
<td>30.86 MHz</td>
<td>7.57 V/µs</td>
</tr>
<tr>
<td>Class A-AB</td>
<td>58.1°</td>
<td>18.3 dB</td>
<td>35.35 MHz</td>
<td>38.8 V/µs</td>
</tr>
<tr>
<td>Full-AB</td>
<td>58.85°</td>
<td>18.42 dB</td>
<td>35.54 MHz</td>
<td>52.55 V/µs</td>
</tr>
</tbody>
</table>

Table 3.14 Topology performance comparison table.
The three topologies were frequency compensated to obtain a phase margin close to 60°. The static power dissipation was set to be close in value for all topologies. The criterion for selecting a frequency compensation capacitor and resistor was to obtain a PM close to 60°. Slew-rate is greater for Full-AB topology, demonstrating the major advantage over the other two topologies.

Figure 3.25 compares the output voltages of the three topologies when a 1Mhz pulse is present at the input. The op-amps were configured as voltage inverters like the one shown in Figure 3.21.

Figure 3.26 shows a closer look of so that the difference in SR between Full-AB and Class A-AB becomes evident.

![Figure 3.25 Output voltage comparison between the three topologies.](image)
Figure 3.26 Closer look at the output voltages.

Figure 3.27 shows the maximum current provided to the compensation capacitor Cc by the first stage of each topology. It is seen that Full-AB can provide more current to this capacitor.

Figure 3.28 and Figure 3.29 show the current sourced and sank by the output transistors Moutp and Moutn of each topology. This plots show that Full-AB op-amp provides the most current to an output load. Finally, a comparison of the maximum current provided to an output load by the three topologies is shown in Figure 3.30.
Figure 3.27 Current in the frequency compensation capacitor, Cc.

Figure 3.28 Current sourced by the PMOS output transistor, Moutp.
Figure 3.29 Current sank by the NMOS output transistor, $M_{outn}$.

Figure 3.30 Current in the output capacitor load, $C_L=20pF$. 


3.4 Hybrid Two Stage Operational Amplifier

The proposed configuration of a Hybrid two-stage op-amp is shown in Figure 3.31. The input differential amplifier used is that proposed in [Ram01] and reviewed in Section 3.1. The second stage is implemented using the differential amplifier proposed in [Pel97] and reviewed in Section 2.2.9.2. The reason that I chose “Hybrid” to be the name of this op-amp is because it is implemented using these two differential amplifiers.

Under quiescent conditions, the current that flows through every transistor of the differential pairs is $I_D$. The differential pairs in the first and second stage are loaded with low-voltage current mirrors M5a, M6a, M7a and M7b, M8b, Moutn respectively. The current that flows in the output transistors Moutp/Moutn is $I_{OUT} = 2*I_D$ as a result of mirroring the current of transistor M6b. Transistors M1a, M2a, M4a, M1b, M2b, M4b and M5b have their bulks connected to their sources in order to eliminate the bulk effect and increase the input CMR.

Assume a differential signal is present at the input of the first stage, for example, a positive $v_{id} = V_{i1} - V_{i2}$. Transistor M2a will source more current than transistor M1a. The voltage at node Y will decrease while node X will be still. As a result, transistor M4b will source more current and transistor M1b will source less current. Transistor Moutp will deliver a large drain current
while transistor \( \text{Moutn} \) will decrease its drain current. Hence, the output voltage \( V_{\text{out}} \) increases. The opposite occurs for a negative input differential signal. When a large differential signal is present at the inputs of the operational amplifier, one of the output transistors will deliver a large current while the other will have a minimum drain current equal to \( I_{\text{MIN}} \). Thus, the configuration shown in Figure 3.31 prevents cut off of the inactive output transistor by biasing it to a minimum drain current equal to \( I_{\text{MIN}} \).

![Figure 3.31 Hybrid operational amplifier.](image)

### 3.4.1 Design procedure for the Hybrid Op-amp

The Hybrid op-amp design is implemented in a MOS 0.5-micron technology. Parameters used for the transistor design were obtained from MOSIS parametric test results for technology SCN05 AMI, http://www.mosis.org. The parameters used in the Hybrid Op-amp design are
summarized in Table 3.1.

3.4.1.1 Design for Input Stage used in the Hybrid Op-Amp

The sizing of transistors M1a, M2a and M4a are exactly the same as the sizing of the corresponding transistors in the Full-AB op-amp shown in Figure 3.8. The transistor sizes for the Hybrid op-amp input stage are shown in Figure 3.32. The bias current sourced by transistors M1a and M2a is $I_D = 100\mu A$. The bias current for M4a is $25\mu A$ and therefore, the bias current for M3a is $225\mu A$.

Transistor M3a width in Figure 3.31 was calculated using a

$$V_{DSatM3a} = 0.13\text{V} :$$

$$W_{3a} = \frac{2 * I_{D3a} * L}{K P p * (V_{DSat3a})^2} = \frac{2 * 225\mu A * 4 \lambda}{38.6 \frac{\mu A}{V^2} * (0.13)^2} \approx 2763\lambda = 829\mu m \quad (3.4.1)$$

This input stage uses a low-voltage implementation current mirror load. The design for transistors M5a and M6a, in Figure 3.31, was done using a $V_{DSat5a,6a} = 0.1V$. This saturation voltage was chosen in order to permit nodes X and Y to have voltage values as low as 0.1 volts and maintain all transistors, in the second stage, in saturation. This consideration is important since the second stage is a differential amplifier with a CMR requirement. Since transistor M7a and 25\mu A-current source inject current to transistors
M5a and M6a, the total bias current sunk by these two transistors is

\[ I_{D5a,6a} = 125 \mu A. \]

\[
(W)_{5a,6a} = \frac{2 * I_{D5a,6a} * L}{K_{Pn} * (V_{DSsat5a,6a})^2} = \frac{2 * 125 \mu A * 4 \lambda}{116 \frac{\mu A}{V^2} * (0.1)^2} \approx 862 \lambda = 258.6\mu m
\]

(3.4.2)

Transistor M7a in Figure 3.31 is designed for a saturation voltage of 0.15V and sources a 25\( \mu \)A current:

\[
(W)_{7a} = \frac{2 * I_{D7a} * L}{K_{Pn} * (V_{DSsat7a})^2} = \frac{2 * 25 \mu A * 4 \lambda}{116 \frac{\mu A}{V^2} * (0.15)^2} \approx 75 \lambda = 22.5\mu m
\]

(3.4.3)

A voltage is applied to the gate of M7a and then the voltage of node X is controlled since it is a gate-to-source voltage below the gate of M7a. Under biasing conditions, the voltage at node Y is the same as node X and since this voltage can be set to a specified value, so can node Y. A desired voltage value for node X and Y under biasing conditions is chosen to be a low voltage in order to maintain the second stage differential amplifier transistors in saturation. However, the voltage at nodes X and Y must not be polarized at such low voltage that the gain of the first stage differential amplifier is degraded.

The bias current circuit that feeds both first and second stage of the
Hybrid op-amp is 25μA. The bias current circuit is shown in Figure 3.33. The same dimensions as the ones calculated for transistor M7a are used for NMOS transistors M1, M2, M3, M8 and M9. PMOS transistors M4, M5, M6 and M7 have a width three times bigger than the width of M7a.

\[
(W)_{4,5,6,7} = (W)_{7a} \times 3 \approx 225 \lambda = 67.5 \mu m
\]  

(3.4.4)

Figure 3.32 Schematic for the input stage used in the Hybrid op-amp.
3.4.1.2 Design for the Input Common-Mode Detector used in the Hybrid Op-Amp

The input common-mode detector used in the Hybrid Op-amp is the same used for the Full-AB op-amp. The design steps for this circuit are given in section 3.3.1.2. The schematic with the corresponding transistor dimensions are shown in Figure 3.9.
3.4.1.3 Design for the Output Stage used in Hybrid Op-Amp

The sizing of transistors M1b, M2b, M4b and M5b, in Figure 3.31, is the same as transistors M1a, M2a and M4a of the first stage. Under biasing conditions, transistors M1b and M4b source a 100\(\mu\)A current. Transistors M2b and M5b source a 25\(\mu\)A current. The transistor dimensions for the second stage are shown in Figure 3.34.

The bias current for transistors M3b and M6b, in Figure 3.31, is 125\(\mu\)A. The widths for these two transistors are calculated with a 0.13V saturation voltage.

\[
(W)_{3b,6b} = \frac{2 \cdot I_{D3b,6b} \cdot L}{KPP \cdot (V_{DSat3b,6b})^2} = \frac{2 \cdot 125\mu A \cdot 3\lambda}{38.6 \frac{\mu A}{V^2} \cdot (0.13)^2} \approx 1104\lambda = 331.2\mu m
\]

(3.4.5)

A 0.9\(\mu\)m \(L = 3\lambda\) length was chosen for transistors M3b and M6b, in Figure 3.31, since the output PMOS transistor, Moutp, is designed for the same length and will copy transistor M6b current. Having both transistors the same length will yield better matching.

NMOS transistor M8b is sized 3 times smaller than transistors M3b or M6b.
\[(W)_{b b} = \frac{(W)_{3b,6b}}{3} \approx 368\lambda = 110.4\mu m \quad (3.4.6)\]

In Figure 3.31, transistor M7b is sized equal to transistor M7a whose dimensions are estimated in equation 3.4.3. A voltage is applied at the gate of transistor M7b and node W is a gate-to-source voltage below it.

Output transistors Moutp and Moutn are sized 2 times bigger than transistors M6b and M8b, respectively. The output bias current is then
\[I_{OUT} = 250\mu A.\]

Figure 3.34 Schematic for the second stage used in the Hybrid op-amp.
3.4.2 Analysis of the Designed Hybrid Op-Amp

In this section the Hybrid operational amplifier designed in Section 3.4.1 is analyzed. A theoretical analysis was done to estimate the Op-amp gain, unity-gain frequency and power consumption under bias conditions. Simulations with BSIM3V3 SPICE models were performed to measure the parameters mentioned above. BSIM3V3 SPICE models are provided in Appendix A. Finally a comparison between theoretical and simulated parameters is provided.

3.4.2.1 Hybrid Op-Amp Gain

In Figure 3.31, nodes Y and Vout are high impedance nodes where the gain of the overall amplifier is determined. Using equations 2.2.23 and 2.2.25 from Chapter 2, the impedance at node Y is calculated. The impedance due to transistors M2a, M6a and the current source (transistor M5 shown in Figure 3.32) is shown in:

\[ r_{o2a} = \frac{1}{\lambda_0 * I_{D2a}} = \frac{1}{0.1 \text{V}^{-1} * 100 \mu A} = 100k\Omega \]  \hspace{1cm} (3.4.7)

\[ r_{o6a} = \frac{1}{\lambda_0 * I_{D6a}} = \frac{1}{0.1 \text{V}^{-1} * 125 \mu A} = 80k\Omega \]  \hspace{1cm} (3.4.8)
\[ r_{o_5} = \frac{1}{\lambda \omega * I_D} = \frac{1}{0.1V^{-1} * 25\mu A} = 400k\Omega \]  

(3.4.9)

\[ R_Y = r_{o_{2a}} || r_{o_{6a}} || r_{o_5} = 40k\Omega \]  

(3.4.10)

The value for channel length modulation, \( \lambda \omega = 0.1V^{-1} \), is selected for MOS transistors with length \( L = 1.2\mu m \).

![Figure 3.35 Impedance at node Y.](image)
The transconductance of transistor $M_{1a}$ in Figure 3.31 is:

\[
gm_{1a} = \sqrt{2 \cdot I_{D1a} \cdot KP \cdot (W)_{1a}/L} = \sqrt{2 \cdot 100 \mu A \cdot 38.6 \frac{\mu A}{V^2} \cdot \frac{921}{4}} = 1.333 \frac{mA}{V}
\]

(3.4.11)

Using equation 2.2.27 in Chapter 2, the gain of the first stage in the circuit shown in Figure 3.7 is calculated.

\[A_1 = gm_{1a} R_Y = 53.32V/V\]  
(3.4.12)

In a similar way, the gain of the output stage is calculated. First the impedance at node $V_{out}$ is estimated:

\[L = 0.9\mu m, \ \lambda_{out} = 0.12V^{-1} \text{ and } I_{Dout} = 278\mu A\]  
(3.4.13)

\[ro_{outn} = ro_{outp} = \frac{1}{\lambda_{out} \cdot I_{Dout}} = \frac{1}{0.12V^{-1} \cdot 278\mu A} = 29.97k\Omega\]  
(3.4.14)

\[R_{out} = ro_{outn} || ro_{outp} = 14.98k\Omega\]  
(3.4.15)

The gain of the output stage is calculated with help of equation 2.2.60 in Chapter 2.

\[
gm_{1b} = \sqrt{2 \cdot I_{D1b} \cdot KP \cdot (W)_{1b}/L} = \sqrt{2 \cdot 100 \mu A \cdot 38.6 \frac{\mu A}{V^2} \cdot \frac{921}{4}} = 1.33 \frac{mA}{V}
\]

(3.4.16)
The mirroring factor between transistor M6b and Moutp or M8b and Moutn is K=2.

\[ A_{OUT} = K \times g_{m_{1b}} \times R_{OUT} = 39.86 \text{V/V} \]  
(3.4.17)

The overall gain is estimated to be:

\[ A_{OL} = A_{i} \times A_{OUT} = 2126 \text{V/V} \]  
(3.4.18)

\[ |A_{OL}| dB = 66.65 dB \]  
(3.4.19)

3.4.2.2 Hybrid Op-Amp Static Power Estimation

To calculate the total static power dissipation in the designed Hybrid Op-amp we first calculate the total current provided by voltage supply \( V_{DD} \).

The total current supplied by \( V_{DD} \) in the input stage of the Hybrid op-amp is shown in Figure 3.32.

\[ I_{STAGE} = 275 \mu A \]  
(3.4.20)

The total current supplied by \( V_{DD} \) in the input common-mode detector of the op-amp is shown in Figure 3.9.

\[ I_{VCM} = 40 \mu A \]  
(3.4.21)
The total current supplied by $V_{DD}$ in the second stage of the Hybrid op-amp is shown in Figure 3.34.

$$I_{2STAGE} = 275 \mu A$$  \hspace{1cm} (3.4.22)

The total current supplied by $V_{DD}$ to the output stage also shown in Figure 3.34 is,

$$I_{OUTPUT} = 250 \mu A$$  \hspace{1cm} (3.4.23)

And considering bias current used in the current mirror circuit that provides current to other stages in the Hybrid Op-amp,

$$I_{CM} = 50 \mu A$$  \hspace{1cm} (3.4.24)

Therefore, the total current supplied by $V_{DD}$ and the total static power dissipated in the Full-AB op-amp are calculated:

$$I_{TOTAL} = I_{1STAGE} + I_{VCM} + I_{2STAGE} + I_{OUTPUT} + I_{CM} = 890 \mu A$$  \hspace{1cm} (3.4.25)

$$P_{STATIC} = I_{TOTAL} \times V_{DD} = 1335 \mu W$$  \hspace{1cm} (3.4.26)

### 3.4.2.3 Simulation Results for the Designed Hybrid Op-amp

Simulations were done using SPICE BSIM3V3 models from a 0.5-micron N-well CMOS technology. SPICE simulation file for Hybrid op-amp is provided in Appendix A.
A DC sweep analysis was performed to estimate the parameters shown in Table 3.15.

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input offset voltage</td>
<td>0.98mV</td>
</tr>
<tr>
<td>Open-loop gain (A_{ol})</td>
<td>1303.8V/V</td>
</tr>
<tr>
<td>A_{ol} dB</td>
<td>62.3dB</td>
</tr>
<tr>
<td>Output voltage swing</td>
<td>1.22V</td>
</tr>
<tr>
<td>Static Power</td>
<td>1326.1\mu W</td>
</tr>
</tbody>
</table>

Table 3.15 DC sweep analysis results.

The test setup used to perform a DC analysis is shown in Figure 3.14 and the output voltage, using this analysis, is shown in Figure 3.36.

DC sweep analysis was also used to demonstrate the output stage Class-AB behavior by monitoring the output transistor currents when a resistive load is applied to the output node.

The test setup is shown in Figure 3.16 and the current transfer characteristic curve is shown in Figure 3.37. It is seen that a minimum current will flow through one of the output transistors while the other is sourcing or sinking a big current. The ratio of the maximum output current to the bias output current is approximately 3. That is small if compared to the ratio found for the Full-AB op-amp where the factor is close to 20, as seen in Figure 3.17.
Figure 3.36 Hybrid op-amp transfer characteristic curve.

A thing to notice about Figure 3.37 is unequal Moutp and Moutn curve shapes. For a negative $V_D$, the output current sunk by Moutn increases until it reaches 0.94mA and then it stays constant. The reason of this is because when current reaches 0.94mA, transistor M3b, in Figure 3.31, is out of saturation and its drain voltage is kept constant. Therefore M1b’s source-to-gate voltage is held constant thus not sourcing more current. On the other hand, for a positive input $V_D$, the output current sourced by Moutp starts
curving down slowly, as compared to Mount current, because its only limitation is in node Y reaching $V_{SS}$.

Figure 3.37 Hybrid op-amp output current transfer characteristic curve.

An AC sweep analysis was performed using the test setup of Figure 3.19 to estimate the parameters shown in Table 3.16.

Frequency compensation circuit is implemented with a capacitor and resistor in series and connected from the output node to Y node. The values that were used for the compensation elements are specified in Table 3.17.
<table>
<thead>
<tr>
<th>Measurement</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Margin</td>
<td>60.27°</td>
</tr>
<tr>
<td>Gain Margin</td>
<td>4.97 dB</td>
</tr>
<tr>
<td>Unity-gain frequency (ft)</td>
<td>24.37MHz</td>
</tr>
<tr>
<td>Open-loop gain (Aol)</td>
<td>1350.6V/V</td>
</tr>
<tr>
<td>Aol dB</td>
<td>62.61 dB</td>
</tr>
</tbody>
</table>

Table 3.16 AC sweep analysis results.

<table>
<thead>
<tr>
<th>Compensation Element</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cc</td>
<td>12pF</td>
</tr>
<tr>
<td>Rz</td>
<td>0.6kOhm</td>
</tr>
</tbody>
</table>

Table 3.17 Frequency compensation circuit.

Figure 3.38 shows a Bode plot of the output voltage including amplitude and phase.

A transient analysis was performed to estimate the parameters shown in Table 3.18.

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR rise</td>
<td>24.2V/μs</td>
</tr>
<tr>
<td>SR fall</td>
<td>24.13V/μs</td>
</tr>
</tbody>
</table>

Table 3.18 Transient analysis results.
The test setup is shown in Figure 3.21 and the transient analysis curves are shown in Figure 3.39. This plot shows an input square voltage signal and the Hybrid op-amp output voltage. This figure also shows currents in the load capacitors as Cload and Cc.

A comparison between theoretical results and simulation results is provided in Table 3.19.
The theoretical estimated open-loop gain is higher than the simulated gain by a factor of 1.6. A situation that affects open-loop gain in Hybrid op-
amp topology is the value selected for $V_{\text{BIAS1}}$ in Figure 3.31. This bias voltage sets the voltage at node X to be $V_{\text{BIAS1}}-V_{\text{GS7a}}$. For a zero differential input to the Hybrid op-amp, node Y is equal to node X. Therefore; $V_{\text{BIAS1}}-V_{\text{GS7a}}$ is the common-mode voltage for the next stage. If $V_{\text{BIAS1}}-V_{\text{GS7a}}$ is small enough, the input stage of the Hybrid op-amp will be operating close the M6a’s $V_{\text{DSsat}}$ hence degrading the overall gain of the op-amp. If $V_{\text{BIAS1}}-V_{\text{GS7a}}$ is high, it may be above the maximum input common mode permitted by the second stage. A possible solution to this problem is the use of QCCFB circuits between the outputs of the first stage to the inputs of the second stage so that nodes X and Y can be set to a value well above M6a’s minimum saturation voltage. This brings the possibility of changing the low-voltage current mirrors like the ones implemented in Figure 3.31 (transistors M5a-M7a and M7b, M8b, Moutn) to a simple current mirror like the one implemented for Full-AB op-amp in Figure 3.7 (transistors M5 and M6).

Unity-gain frequency, $f_u$, is higher in the simulation than estimated from theory. The theoretical estimation was done using equation 3.3.52. The zero location in the bode plot shown in Figure 3.38 helps the Hybrid op-amp to achieve a better unity-gain frequency in simulation.

Slew-rate result is lower than the initial specification of 47V/µs. In Chapter 2, equation 2.2.53 was derived for slew-rate in a two-stage op-amp. The result is shown again in equation 3.4.27.
This equation suggests that slew-rate depends on the maximum current that the Hybrid op-amp first stage can provide to capacitor $C_C$. In the case of a simple two-stage op-amp, the maximum current that can be provided to $C_C$ is the differential pair's tail current, $I_{SS}$. For the Hybrid op-amp, the maximum current that can be provided to $C_C$ is between 3 to 5 times the bias current. The Full-AB op-amp is also able to provide 3 to 5 times the bias current to $C_C$. Comparing the compensation capacitor, $C_C$, used in the Hybrid op-amp to the one used Full-AB op-amp, the difference ratio is 2.13. If we compare slew-rate between the two topologies, the difference ratio is 2.72.
4 HARDWARE TESTING AND LAYOUT

This chapter presents experimental results on the Full-AB and Hybrid two stage op-amp topologies. The ICs were fabricated using the 0.5\(\mu\)m AMI n-well process. An important note that must be taken into consideration is that the laid out ICs are entirely based on the design presented in [Ram01]. What needs to be understood from this is that transistor dimensions used are the ones shown in [Ram01] and not the ones obtained in Chapter 3. Chapter 3 designs, even though based on [Ram01], take into account the specifications showed in Section 3.3.1; thus, transistor dimensions are different. Experimental results for three different topologies are presented in this chapter. The first two circuits are Full-AB and Hybrid op-amps described in Chapter 3. The third circuit is a variation of the Hybrid op-amp and is described in the following sections. This chapter starts with a review of the different tests performed with the ICs. After the review, results for the specific topology are presented. Layout is also shown for each circuit.

4.1 Hardware Test Setup

Three different parameters are tested in the fabricated ICs in order to compare results against simulated results. The parameters are slew-rate, input-to-output transfer characteristic and unity-gain frequency.
The test setup used to measure slew-rate and output range is shown in Figure 4.1 and based on [Car00].

![Figure 4.1 Low power-supply inverting configuration.](image)

The test setup based on Figure 4.1 is shown completely in Figure 4.2.

![Figure 4.2 Slew rate and output range test setup.](image)
The signal generator is an HP 33120A. A square wave is used for slew-rate measurements. For the experiment a 1.5Vp-p, 0.75V dc offset, 200kHz-square wave like the one shown in Figure 4.3 were used.

![Graph showing a 200kHz square wave generated with 33120A.](image)

**Figure 4.3** 200kHz square wave generated with 33120A.

For input-to-output transfer characteristic, a 50Hz-triangular signal is used like the one shown in Figure 4.4.

The 0.6V battery in Figure 4.1 is implemented with a DC voltage source such as an E3630A or a drained 9 V battery.
The measurement device used is a 54645D Oscilloscope and a 10073C passive probe. A DC power box available at the lab provides DC voltages needed by the IC.

Figure 4.4 50-Hz triangular signal generated by 33120A.

The test setup used to measure unity-gain bandwidth is shown in Figure 4.5. And the complete test setup is shown in Figure 4.6.
Figure 4.5 Voltage follower configuration.

The 0.6V is no longer needed and the feedback connection in the op-amp changes from resistors to a direct feedback. The input test signal is a 200mVp-p sinusoidal signal, superimposed on a 0.15V offset, sinusoidal signal at a frequency that will cause the op-amp output to be $\frac{1}{\sqrt{2}}$ or 3dB down with respect to the input signal. In this case the desired outcome will be the signal frequency that generates an output amplitude of 141.42mVp-p. The input test signal used is shown in Figure 4.7.

Figure 4.6 Unity-gain frequency test setup.
4.2 Full-AB Op-Amp Experimental Results

A schematic for a Full-AB two-stage op-amp was shown in Chapter 3, section 3.3. The schematic is shown again in Figure 4.8. Also circuit schematics for the input common-mode voltage and for QCCFB are shown in Figure 4.9 and Figure 4.10. The transistor sizes, bias currents and voltages, which are used for the input and common-mode voltage, are shown in Table 4.1 and Table 4.2. Tables 4.3, 4.4 and 4.5 summarize QCCFB. Full-AB op-amp chip pin-out table is available in Appendix B.
Figure 4.8 Full-AB Operational amplifier.

<table>
<thead>
<tr>
<th>Input Stage</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>400µm</td>
<td>1.2µm</td>
</tr>
<tr>
<td>M2</td>
<td>400µm</td>
<td>1.2µm</td>
</tr>
<tr>
<td>M3</td>
<td>400µm</td>
<td>1.2µm</td>
</tr>
<tr>
<td>M4</td>
<td>400µm</td>
<td>1.2µm</td>
</tr>
<tr>
<td>M5</td>
<td>801µm</td>
<td>1.2µm</td>
</tr>
<tr>
<td>M6</td>
<td>801µm</td>
<td>1.2µm</td>
</tr>
<tr>
<td>Bias</td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>IB</td>
<td></td>
<td>15µA</td>
</tr>
</tbody>
</table>

Table 4.1 Full-AB op-amp; input stage transistor sizing and bias.
Figure 4.9 Common mode voltage detector.

Table 4.2 Full-AB op-amp; input common-mode voltage detector transistor sizing and bias.

<table>
<thead>
<tr>
<th>CMV detector</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>40.2µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M2</td>
<td>40.2µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M3</td>
<td>40.2µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M4</td>
<td>40.2µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>Bias</td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>Ib2'</td>
<td></td>
<td>4µA</td>
</tr>
</tbody>
</table>
Figure 4.10 Quiescent current controlled floating battery (QCCFB).

<table>
<thead>
<tr>
<th>Bias</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Id</td>
<td>4μA</td>
</tr>
<tr>
<td>I1</td>
<td>2μA</td>
</tr>
<tr>
<td>$V_{BIASN}$</td>
<td>1.3V</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>1.5V</td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>0V</td>
</tr>
</tbody>
</table>

Table 4.3 QCCFB Biasing.
<table>
<thead>
<tr>
<th>QCCFB</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>6µm</td>
<td>2.1µm</td>
</tr>
<tr>
<td>M2</td>
<td>4.2µm</td>
<td>2.1µm</td>
</tr>
<tr>
<td>M3</td>
<td>3µm</td>
<td>2.1µm</td>
</tr>
<tr>
<td>M4</td>
<td>2.1µm</td>
<td>2.1µm</td>
</tr>
<tr>
<td>M5</td>
<td>3µm</td>
<td>2.1µm</td>
</tr>
<tr>
<td>M6</td>
<td>2.1µm</td>
<td>2.1µm</td>
</tr>
<tr>
<td>M7</td>
<td>2.1µm</td>
<td>2.1µm</td>
</tr>
<tr>
<td>M8</td>
<td>3µm</td>
<td>2.1µm</td>
</tr>
<tr>
<td>M9</td>
<td>2.1µm</td>
<td>2.1µm</td>
</tr>
<tr>
<td>M10</td>
<td>60µm</td>
<td>1.2µm</td>
</tr>
<tr>
<td>M11</td>
<td>60µm</td>
<td>1.2µm</td>
</tr>
</tbody>
</table>

Table 4.4 QCCFB transistor sizing, bias and frequency compensation network.

<table>
<thead>
<tr>
<th>Passive Element</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cc</td>
<td>20pF</td>
</tr>
<tr>
<td>Rz</td>
<td>1kOhm</td>
</tr>
<tr>
<td>Cc2</td>
<td>1pF</td>
</tr>
<tr>
<td>R</td>
<td>150kOhm</td>
</tr>
</tbody>
</table>

Table 4.5 Passive elements used in QCCFB.
4.2.1 Slew-Rate Measurement for Full-AB Op-Amp

Figure 4.11 Slew-rate experimental results for Full-AB op-amp.

Figure 4.11 shows the input signal used for the test plus a simulated output voltage and a measured voltage. When the output signal toggles from high to low, the simulated result is similar to the experimental result, even though the latter has more delay. On the other hand, when the output signal changes from low to high level, the simulated output has a considerably larger slew-rate. A quantitative measure is shown in Table 4.6.
<table>
<thead>
<tr>
<th>Slew rate (SR)</th>
<th>SR rise</th>
<th>SR fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulated result</td>
<td>3.918V/µs</td>
<td>16.54V/µs</td>
</tr>
<tr>
<td>Experimental result</td>
<td>3.16V/µs</td>
<td>5.25V/µs</td>
</tr>
</tbody>
</table>

Table 4.6 Slew-rate simulated vs. experimental results.

4.2.2 Input to Output Measurement for Full-AB Op-Amp

![Graph](image)

Figure 4.12 Full-AB input/output transference characteristic.

Figure 4.12 shows the output voltage when the input is swept from 0 to 1.5V. The slopes of a simulated and experimental input/output transference characteristic are close to 1.
4.2.3 Full-AB Op-Amp Bandwidth

Figure 4.13 shows the unity-frequency bandwidth obtained from simulation. The value for unity-gain bandwidth obtained in simulation is $f_t = 2.4 \text{MHz}$.

Figure 4.13 Full-AB simulated Bode plot of open-loop gain.

Figure 4.14 shows laboratory results to measure unity-frequency bandwidth. The input signal frequency that makes the output voltage to be 3dB down with respect to the input, unity-gain bandwidth, is $f_t = 2.25 \text{MHz}$. 

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4.2.4 Full-AB Op-Amp Summary Results

Three chips were tested in laboratory and results are summarized in Table 4.7.

<table>
<thead>
<tr>
<th></th>
<th>SR rise</th>
<th>SR down</th>
<th>Unity-gain bandwidth (f_i)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip 1</td>
<td>3.16 V/µs</td>
<td>5.25V/µs</td>
<td>2.25MHz</td>
</tr>
<tr>
<td>Chip 2</td>
<td>3.01 V/µs</td>
<td>5.29V/µs</td>
<td>1.83MHz</td>
</tr>
<tr>
<td>Chip 3</td>
<td>2.87 V/µs</td>
<td>4.79V/µs</td>
<td>1.74MHz</td>
</tr>
<tr>
<td>Full-AB Simulation</td>
<td>3.93 V/µs</td>
<td>1.65V/µs</td>
<td>2.41MHz</td>
</tr>
</tbody>
</table>

Table 4.7 Hardware measurement results for the Full-AB op-amp.
4.2.5 Full-AB Op-Amp Layout

Figure 4.15 shows the complete layout for Full-AB op-amp. The layout includes frequency compensation capacitors and a resistor. Capacitors are made with poly1-poly2 layers. Resistor is made with the poly1 layer. Also included in the layout are two resistors needed for the QCCFB circuit, also implemented with the poly1 layer.

As shown in the figure, the compensation capacitor occupies a considerable amount of area since its value is 20pF. Careful design of the first and second stages in the two-stage amplifier may bring down the value of the compensation capacitor, thus, reducing the occupied area.

To estimate the area needed for the 20pF compensation capacitor, the following formula was used:

\[ C_c = C_{\text{PER-SQUARE}} \times A_{\text{CAP}} \]  

(4.1)

\( C_{\text{PER-SQUARE}} \) is the capacitance, in this case, between poly1-poly2 layers per squared micron. This information can be obtained in a 0.5\( \mu \text{m} \) AMI n-well process parametric test result provided by MOSIS. In this case we use t13v run and \( C_{\text{PER-SQUARE}} = 929 \text{aF/} \mu \text{m}^2 \). Solving for area yields:

\[ A_{\text{CAP}} = C_c / C_{\text{PER-SQUARE}} = 21528 \mu \text{m}^2 \]  

(4.2)

Same procedure was followed for \( C_c2=1\text{pF} \).
Resistors can be implemented using poly2 and high resistance layers. In this way, resistors will not occupy as much area as the one occupied in Figure 4.15. Another note on this is that R=150Kohm. Careful design of QCCFB will yield small values for the two resistors needed and, therefore, occupy less area.

To estimate the area needed for R=150kOhm, the following formula is used:

$$ R = R_{SQ} \frac{L}{W} \quad (4.3) $$

$R_{SQ}$ is the sheet resistance per square, in this case, using the poly1 layer. This value was obtained from t13v run to be equal to 23.0 ohms. The minimum width for poly 1 is $W=0.6 \mu m$. Solving for R yields:

$$ L = W \cdot \frac{R}{R_{SQ}} = 3913 \mu m \quad (4.4) $$

$L$ was divided into 15 segments of 260$\mu m$ length. These segments are joined together in series to obtain the required resistance value. Same procedure was used to implement 1Kohm, $R_z$.

$$ L_z = W \cdot \frac{R_z}{R_{SQ}} = 26 \mu m \quad (4.5) $$

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A closer look to the layout is shown in Figure 4.16. Here some of the transistors are shown. The bulk connections for PMOS and NMOS transistors are laid out surrounding the circuit. These bulk connections are then connected to $V_{DD}$ and $V_{SS}$ in the chip. Bulk connection layers are thick and have metal-to-active connections through the layers.
Layouts should be close to a square figure as possible. This helps optimize area in a chip hence, allowing more circuits in less area. Obviously Figure 4.16 is far from being square in shape.

4.3 Hybrid Op-Amp Experimental Results

The circuit schematic is shown in Figure 4.17. The input common mode detector is the same as that shown in Figure 4.9.
Figure 4.17 Hybrid op-amp circuit schematic.

The bias elements and transistor sizes for input stage are shown in Table 4.8 and Table 4.9 respectively. Transistor sizes and biasing for CMV are shown in Table 4.10. Transistor sizes and biasing elements used for the second stage of the circuit shown in Figure 4.17 are provided in Table 4.11. Passive elements used in circuit shown in Figure 4.17 are provided in Table 4.12. Hybrid op-amp chip pin-out is available in Appendix B.

<table>
<thead>
<tr>
<th>Bias</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BIASN1}$</td>
<td>1.1V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>3µA</td>
</tr>
</tbody>
</table>

Table 4.8 Hybrid op-amp, input stage bias.
### Table 4.9 Hybrid op-amp; input stage transistor sizes.

<table>
<thead>
<tr>
<th>Input stage</th>
<th>Width (μm)</th>
<th>Length (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1a</td>
<td>100.8μm</td>
<td>1.5μm</td>
</tr>
<tr>
<td>M2a</td>
<td>100.8μm</td>
<td>1.5μm</td>
</tr>
<tr>
<td>M3a</td>
<td>302.4μm</td>
<td>1.5μm</td>
</tr>
<tr>
<td>M4a</td>
<td>100.8μm</td>
<td>1.5μm</td>
</tr>
<tr>
<td>M5a</td>
<td>36μm</td>
<td>1.5μm</td>
</tr>
<tr>
<td>M6a</td>
<td>36μm</td>
<td>1.5μm</td>
</tr>
<tr>
<td>M7a</td>
<td>36μm</td>
<td>1.5μm</td>
</tr>
</tbody>
</table>

### Table 4.10 Hybrid op-amp; input common-mode voltage detector transistor sizes and bias.

<table>
<thead>
<tr>
<th>CMV detector</th>
<th>Width (μm)</th>
<th>Length (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>10.8μm</td>
<td>1.5μm</td>
</tr>
<tr>
<td>M2</td>
<td>10.8μm</td>
<td>1.5μm</td>
</tr>
<tr>
<td>M3</td>
<td>10.8μm</td>
<td>1.5μm</td>
</tr>
<tr>
<td>M4</td>
<td>10.8μm</td>
<td>1.5μm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bias</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ib2’</td>
<td>0.8μA</td>
</tr>
</tbody>
</table>

Table 4.9 Hybrid op-amp; input stage transistor sizes.

Table 4.10 Hybrid op-amp; input common-mode voltage detector transistor sizes and bias.
<table>
<thead>
<tr>
<th>Second stage</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1b</td>
<td>100.8µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M2b</td>
<td>100.8µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M3b</td>
<td>302.4µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M4b</td>
<td>100.8µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M5b</td>
<td>100.8µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M6b</td>
<td>302.4µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M7b</td>
<td>36µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M8b</td>
<td>36µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>Moutp</td>
<td>907.2µm</td>
<td>0.9µm</td>
</tr>
<tr>
<td>Moutn</td>
<td>108µm</td>
<td>0.9µm</td>
</tr>
<tr>
<td><strong>Bias</strong></td>
<td><strong>Value</strong></td>
<td></td>
</tr>
<tr>
<td>$V_{BIAASN2}$</td>
<td>1.3V</td>
<td></td>
</tr>
<tr>
<td>$I_D$</td>
<td>3µA</td>
<td></td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>45µA</td>
<td></td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>1.5V</td>
<td></td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>0V</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.11 Hybrid op-amp; second stage transistor sizing and bias.
A variation of the Hybrid op-amp circuit reviewed in Chapter 3, Section 3.4 is shown in Figure 4.18 and Figure 4.19. The basic difference is that it uses an input stage based on the topology reviewed in Chapter 2, Section 2.2.9.2. The first and second stages used the same topology. I decided to call it, Hybrid-2 op-amp.
The transistor sizes and bias currents and voltages for input stage are shown in Table 4.13. Bias elements for the second stage of Hybrid-2 op-amp are shown in Table 4.14. Transistor sizes and passive elements for the second stage of Hybrid-2 op-amp are shown in Table 4.15. Hybrid-2 op-amp chip pin-out is available in Appendix B.

<table>
<thead>
<tr>
<th>Input stage</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1a</td>
<td>100.8 µm</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>M2a</td>
<td>100.8 µm</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>M3a</td>
<td>302.4 µm</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>M4a</td>
<td>100.8 µm</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>M5a</td>
<td>100.8 µm</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>M6a</td>
<td>302.4 µm</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>M7a</td>
<td>36 µm</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>M8a</td>
<td>36 µm</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>M9a</td>
<td>36 µm</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>Bias</td>
<td>Value</td>
<td></td>
</tr>
<tr>
<td>$V_{BIASN1}$</td>
<td>1.1V</td>
<td></td>
</tr>
<tr>
<td>$I_D$</td>
<td>3 µA</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.13 Hybrid-2 op-amp; input stage transistor sizing and bias.
Figure 4.19 Hybrid-2 op-amp output stage.

<table>
<thead>
<tr>
<th>Bias</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BIASN2}$</td>
<td>1.3V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>3µA</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>45µA</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>1.5V</td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>0V</td>
</tr>
</tbody>
</table>

Table 4.14 Hybrid-2 op-amp; bias elements.
<table>
<thead>
<tr>
<th>Second stage</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1b</td>
<td>100.8µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M2b</td>
<td>100.8µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M3b</td>
<td>302.4µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M4b</td>
<td>100.8µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M5b</td>
<td>100.8µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M6b</td>
<td>302.4µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M7b</td>
<td>36µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>M8b</td>
<td>36µm</td>
<td>1.5µm</td>
</tr>
<tr>
<td>Moutp</td>
<td>907.2µm</td>
<td>0.9µm</td>
</tr>
<tr>
<td>Moutn</td>
<td>108µm</td>
<td>0.9µm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Passive element</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cc</td>
<td>8pF</td>
</tr>
<tr>
<td>Rz</td>
<td>2kOhm</td>
</tr>
</tbody>
</table>

Table 4.15 Hybrid-2 op-amp; second stage transistor sizing and passive elements.

### 4.3.1 Slew-Rate Measurement for Hybrid Op-Amp

Slew rate measurement results are shown in Figure 4.20 and Table 4.16 for the Hybrid op-amp. Hybrid op-amp results show similar results compared to the simulated circuit.
The measured output has a considerable delay in comparison to the simulated output, similar to the results for the Full-AB op-amp.

![Slew-rate experimental results for Hybrid op-amp.](image)

**Figure 4.20** Slew-rate experimental results for Hybrid op-amp.

<table>
<thead>
<tr>
<th>Slew-rate (SR)</th>
<th>SR rise</th>
<th>SR fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulated result</td>
<td>5.3V/µs</td>
<td>5.44V/µs</td>
</tr>
<tr>
<td>Experimental</td>
<td>4.01V/µs</td>
<td>6.82V/µs</td>
</tr>
</tbody>
</table>

Table 4.16 Slew-rate simulated vs. experimental results for the Hybrid op-amp.
Experimental results for the Hybrid-2 are shown in Figure 4.21 and Table 4.17. The simulated output, when toggling from high level to low, presents a slew-rate three times higher than that of measured output. There is a delay between the measured output and the simulated output voltage.

![Figure 4.21 Slew-rate experimental results for the Hybrid-2 op-amp.](image)

<table>
<thead>
<tr>
<th>Slew-rate (SR)</th>
<th>SR rise</th>
<th>SR fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulated result</td>
<td>17.3V/\mu s</td>
<td>4.91V/\mu s</td>
</tr>
<tr>
<td>Experimental result</td>
<td>5.2V/\mu s</td>
<td>5.92V/\mu s</td>
</tr>
</tbody>
</table>

Table 4.17 Slew-rate simulated vs. experimental results for the Hybrid 2 op-amp.
4.3.2 Input to output measurement for Hybrid Op-Amp

Figure 4.22 Hybrid input/output transfer characteristic.

Figure 4.22 shows the input/output transfer characteristic when the Hybrid op-amp is configured as a low-voltage amplifier. It is shown how the output voltage change from 1.5 V to 0 as the input voltage sweeps from 0 to 1.5 V. The measured output is similar to the simulated version. Slopes of the two plots are close in value. Figure 4.23 shows the input/output transfer characteristic of Hybrid-2 op-amp. A similar result is obtained for Hybrid-2 op-amp.
4.3.3 Hybrid Op-Amp Bandwidth

Figure 4.24 shows the simulated unity-gain frequency for the Hybrid and Hybrid-2 op-amps. Figure 4.25 and Figure 4.26 show results for measured unity-gain frequency. Measured results for the Hybrid op-amp are very close to simulated result. On the other hand, measured results for the Hybrid-2 are almost twice the simulated result.
Figure 4.24 Hybrid and Hybrid-2 simulated bode plots.

Figure 4.25 Hybrid bandwidth test measurement.
4.3.4 Hybrid Op-Amp Summary of Results

<table>
<thead>
<tr>
<th></th>
<th>SR rise</th>
<th>SR down</th>
<th>Unity-gain frequency ($f_t$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip 1</td>
<td>4.01V/µs</td>
<td>6.82V/µs</td>
<td>3.68MHz</td>
</tr>
<tr>
<td>Chip 2</td>
<td>4.55V/µs</td>
<td>7.61V/µs</td>
<td>4.31MHz</td>
</tr>
<tr>
<td>Chip 3</td>
<td>4.14V/µs</td>
<td>7.48V/µs</td>
<td>4.35MHz</td>
</tr>
<tr>
<td>Hybrid Simulation</td>
<td>5.3 V/µs</td>
<td>5.44V/µs</td>
<td>3.47MHz</td>
</tr>
</tbody>
</table>

Table 4.18 Hardware measurement results for the Hybrid op-amp.
### Table 4.19 Hardware measurement results for the Hybrid-2 op-amp.

<table>
<thead>
<tr>
<th></th>
<th>SR rise</th>
<th>SR down</th>
<th>Unity-gain frequency ($f_t$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip 1</td>
<td>5.20V/µs</td>
<td>5.92V/µs</td>
<td>4.39MHz</td>
</tr>
<tr>
<td>Chip 2</td>
<td>4.44V/µs</td>
<td>5.32V/µs</td>
<td>4.72MHz</td>
</tr>
<tr>
<td>Chip 3</td>
<td>4.4V/µs</td>
<td>4.93V/µs</td>
<td>4.67MHz</td>
</tr>
<tr>
<td>Hybrid-2</td>
<td>17.3V/µs</td>
<td>4.91V/µs</td>
<td>2.55MHz</td>
</tr>
</tbody>
</table>

#### 4.3.5 Hybrid Op-Amp Layout

The layout for the Hybrid op-amp is shown in Figure 4.27. As can be seen from the figure, I tried to maintain the shape as square as possible. An effort was put into minimizing the height of the layout. To keep the height as small as possible will help avoid latch-up effect that may occur in a practical situation [Bak98]. The width of the layout on the other hand is big. If we compare Figure 4.27 to Figure 4.15 we see that the former is easier to place on a chip that contains other circuits due to its shape. Figure 4.15 has a very irregular shape that may interfere with other circuits on a chip, especially if almost all of the area on the chip is occupied.

The frequency compensation capacitor and resistor were designed using the same method as the one explained in section 4.2.5. However, the resistor was laid out using the poly2 high resistance layer. To build a resistor...
using this method, a poly-2 layer and high resistor mask on top of it must be used. The sheet resistance for the combination of these two layers is 946 ohms per square. For example, the 6kOhm zero canceling resistor requires a layout length of:

\[ L_z = W \times \frac{R_z}{R_{\text{HIGHRES \_ SQUARE}}} = 13.31\mu m \]  \hspace{1cm} (4.6)

\[ W = 7\lambda = 2.1\mu m \]  \hspace{1cm} (4.7)

If we compare the result in equation 4.6 to 4.5 it is seen that half the length is used for a resistor that is 6 times bigger.

The layout for the Hybrid-2 op-amp is shown in Figure 4.28. The same methodology was used for the Hybrid-2 op-amp as for the Hybrid op-amp.
Figure 4.29 shows a closer look at the Hybrid-2 op-amp. In this figure several things can be noticed. Inter-digitation techniques were used in order to avoid manufacturing limitations that create mismatches between transistor dimensions. The transistors were laid out as close as possible to each other to maintain the area as small as possible. PMOS transistors were placed on top and NMOS transistors were placed on the bottom. A PMOS bulk connection ring was placed around the PMOS devices. The same method was followed for the NMOS bulk connection ring that surrounded NMOS devices. The NMOS bulk connection ring also surrounds the PMOS bulk connection ring. The PMOS bulk connection is tied to $V_{DD}$ and the NMOS bulk connection ring is tied to $V_{SS}$ on the chip. Having bulk connection rings surrounding the devices helps to keep out any potential noisy signals created outside the op-amp and created by circuits located close to op-amp.

When the layout was built, I separated the circuit schematic into first, second and output stages. The second stage is the class AB differential pair that follows to the input stage. The output stage consists of the PMOS and NMOS transistors that drive an external load. I laid out all the PMOS devices together for a particular stage and then surrounded them with their bulk connection ring. The same method was done with all NMOS devices for a particular stage. After this I joined the PMOS and NMOS devices and their bulk connection rings to layout the particular stage. I continued using this
method for the subsequent stages. At the end, I pieced together the complete op-amp architecture. Following this method made it hard to wire some of the nodes, specifically when connecting PMOS devices to the NMOS devices in the particular stages. Eliminating the use of bulk connection rings could help avoid wiring issues and perhaps allow transistor devices to be placed closer to each other, with the trade-off of lower noise immunity and potential latch-up of the circuit.

Figure 4.29 Closer look of the Hybrid-2 op-amp.
5 CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

This chapter is divided into several sections that discuss low-voltage design considerations, a comparison between the proposed topologies and the solutions that exist in literature and were reviewed in Chapter 2. This chapter also provides discussion on the results for the topology comparison performed in Chapter 3 as well as the experimental results shown in Chapter 4. Finally, this conclusions chapter provides recommendations for future research in low-voltage schemes.

5.1.1 Low-Voltage Design Considerations

Low-voltage design requires a very good understanding of basic analog building block circuits such as output stages and operational amplifiers. Reducing voltage supply to its minimal possible value requires refined design and testing techniques.

For example, the input common voltage range becomes very small when biasing the op-amp at low voltages such as 1.5V. The input common voltage range calculated for Full-AB op-amp is from 0 to 0.3V, as shown in Section 3.3.2.1, Chapter 3. If we bias the op-amp at an input common voltage
outside this range, we will pull some of the transistors, in the op-amp, out of saturation and the circuit will malfunction. When a circuit is biased with higher supply levels, the input common voltage is bigger and you may not run with this problem may not occur.

Another factor that becomes important when you use a single low-voltage supply is how the entire circuit in a specific configuration is biased. Op-amps fed with higher voltage supplies commonly use bipolar supplies, i.e. ±2.5V. A schematic of an op-amp configured as a voltage inverter and using a bipolar supply voltage such as ±2.5V is shown in Figure 5.1. The input common voltage is set to 0 since this level is included in the input common voltage range. The same situation occurs for the output common mode voltage in, it is 0 volts since it is in the middle of ±2.5V supplies.

![Figure 5.1 Voltage inverter configuration.](image)

On the other hand, low-voltage op-amps powered by a single supply
must use a configuration that will set an input common-mode close to one of the voltage rails. In the case of the designs presented in Chapter 3, we kept the input common-mode voltage close to 0, since we are using PMOS devices for the input differential amplifier. If we had used NMOS devices, the input common-mode voltage would have been kept at a level close to single power supply, in this case 1.5V. The output common-mode voltage is kept at the power supply middle level, in our case 0.75V. A voltage inverter configuration that satisfies the requirements mentioned above is shown in Figure 5.2.

![Figure 5.2 Low-voltage inverter configuration.](image)

Figure 5.2 adds complexity to the simple voltage inverter since it needs a 0.15V at the positive op-amp input terminal and a 0.6V floating battery. A principle used for QCCFB circuit in Section 3.2, Chapter 3, can be used to implement this 0.6V floating battery as is proposed in [Ram98]. In our case,
in Chapter 4, we didn’t consider this situation until it was too late and we already had a physical chip without the 0.6V floating battery implementation circuit. We used a worn-out battery instead that had a value close to 0.6V.

Op-amps were designed to work at relatively high speeds but using low supplies. The result was increased transistor dimension sizes since the minimum saturation voltages were chosen around 0.1V and currents were in the range of 25uA to 1mA. Area increases as low voltages increases and high speed is desired.

The other factor that increases layout area is that the bulk of the transistors in the differential amplifier must be connected to their sources. This decreases the effective gate-to-source voltages of the transistors in question but requires an extra connection to bulk in layout. This takes a considerable amount of layout area.

5.1.2 Comparison of the Proposed Circuit Architectures with the Topologies Existing in the Literature

In Chapter 2, a few Class AB topologies that exist in literature were reviewed. Each reviewed topology has advantages and disadvantages, which are mentioned in Table 5.1.
<table>
<thead>
<tr>
<th>Topology</th>
<th>Reviewed in section:</th>
<th>Advantage</th>
<th>Disadvantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class AB output stage based on a complementary head to tail connected transistors [Was99]</td>
<td>2.1.3.1</td>
<td>Achieves accurate quiescent current control.</td>
<td>It requires high voltage supply, $3V_{DSsat}+2V_{TH}$.</td>
</tr>
<tr>
<td>Low-voltage class AB buffers with quiescent current control [You98]</td>
<td>2.1.3.2</td>
<td>The proposed circuit is very simple and easy to implement. Low voltage supply $2V_{DSsat}+V_{TH}$.</td>
<td>Dependence on process variations is not fully eliminated.</td>
</tr>
<tr>
<td>Low-voltage feedback class AB output stage with minimum selector [Lan98]</td>
<td>2.1.3.3</td>
<td>Achieves accurate quiescent current control at low voltage supply, $3V_{DSsat}+V_{TH}$.</td>
<td>Design and implementation is more involved. It has a feedback loop that may cause slower speed and stability problems.</td>
</tr>
<tr>
<td>Low voltage class AB output stage with quiescent current control floating battery. QCCFB [Car00]</td>
<td>3.2</td>
<td>Achieves accurate quiescent current control at low voltage supply, $2V_{DSsat}+V_{TH}$. The quiescent current can be controlled and set to any value in a valid range.</td>
<td>Even though design is not as difficult as [Lan98], it still adds some complexity to the design. In contrast to the other topologies, QCCFB circuit makes use of resistors, which occupy wafer area.</td>
</tr>
</tbody>
</table>

Table 5.1 Class AB output stages advantages and disadvantages.
Chapter 2 includes a review of class AB input stages that exist in literature. Each reviewed topology has advantages and disadvantages, which are mentioned in Table 5.2.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Reviewed in section:</th>
<th>Advantage</th>
<th>Disadvantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source Cross-Coupled Pair [Cas85]</td>
<td>2.2.9.1</td>
<td>Good class AB performance.</td>
<td>High voltage supply requirement, $3V_{DSat}+2V_{TH}$. Reduced effective transconductance, which degrades bandwidth performance.</td>
</tr>
<tr>
<td>A topology based on the use of flipped voltage followers [Pel97]</td>
<td>2.2.9.2</td>
<td>Good class AB performance at low voltage supply requirement, $2V_{DSat}+V_{TH}$.</td>
<td>Increased dynamic (transient) voltage supply requirement, $V_{SUP}=V_{SGQ}+V_{DSatQ}+2V_{Dmax}$.</td>
</tr>
<tr>
<td>Proposed class AB differential amplifier [Ram01]</td>
<td>3.1</td>
<td>Good class AB performance at low voltage supply requirement, $2V_{DSat}+V_{TH}$. Lower dynamic (transient) supply requirement, in contrast to Peluso [Pel97]: $V_{SUP}=V_{SGQ}+V_{DSatQ}+V_{Dmax}$.</td>
<td>This class AB input requires a common-mode sensing network, [Joh97] which adds more transistors to the implementation.</td>
</tr>
</tbody>
</table>

Table 5.2 Class AB input stages advantages and disadvantages.
5.1.3 Results for the Proposed Topologies

In Chapter 3, a Full-AB op-amp was designed which consists of a Ramirez-Angulo [Pel97] class AB input differential amplifier and a QCCFB [Car00] Class AB output stage. Some initial design specifications were determined and the design started from there.

The Full-AB op-amp final design exceeds the initial specs. The unity-gain bandwidth specified (GBW) is 20Mhz against a simulated GBW of 35.54MHz. The specified Slew-rate (SR) for a 20pF load is 47V/μs while in simulation it was proven that the designed Full-AB op-amp has a SR of 52.23V/μs for the specified load.

To prove that the Full-AB op-amp has a SR improvement over a class A two-stage op-amp (Full-A) and a class A input, Class-AB output stage op-amp (Class A-AB), simulation results were compared. The results are presented in Chapter 3, Section 3.3.2.4. To make sure a fair comparison was made, Full-A and Class A-AB op-amps were designed to match the same static power dissipation. Class A-AB uses a class A input differential amplifier and the same second stage (QCCFB plus output transistors) as used for the Full-AB op-amp. It is shown that the Full-AB op-amp has a SR that is 6.9 times larger than the Full-A SR and 1.34 times larger than the Class A-AB
SR. To achieve a 52.23V/\mu s SR using the Full-A op-amp, an increase of 330% in the static power dissipation is required. To achieve a 52.23V/\mu s SR using the Class A-AB op-amp, a 33.5% increase in the static power dissipation is required.

In Chapter 3, a second topology was proposed and was denoted Hybrid op-amp since it uses a Ramirez-Angulo [Pel97] class AB input differential amplifier and a Peluso [Pel97] class AB differential amplifier implemented as the second stage of the op-amp. Since both differential amplifiers were built with PMOS devices and require a common-mode input voltage close to V_{SS} rail, I used low-voltage current mirrors as active loads for the first and second stages. A disadvantage of using this low-voltage current mirrors is that they require extra biasing currents that increment the overall static power dissipation. Special attention must be paid to the common-mode output voltage level of the first stage so that the second stage is operating with all its transistors in saturation.

The Hybrid op-amp SR obtained in simulation was 20.9V/\mu s, which is 2.5 times smaller than the SR of the Full-AB op-amp. The aspect ratio between the output quiescent current and the maximum current sourced or sank by one of the output transistors is 2.5. On the other hand, for the Full-AB op-amp this ratio is close to 12.
5.1.4 Experimental Results

Chapter 4 presented results for physical implementation of the proposed topologies. The ICs were fabricated using the 0.5\,\mu m AMI n-well process. The experimental results were compared to simulations and similarity between them was found. Some experimental results for SR measurement show a delay that is not seen in simulation.

Layout was shown for every op-amp. An increase in layout skills between the first laid-out chip to the last is evident. The layout of my first chip does not occupy area efficiently because I did not put attention into making the layout close to a square shape. I came up with huge resistor values that I implemented with poly layer and occupied an incredible amount of area. As can be seen for the other 2 layouts, they have a more rectangular shape, occupying area efficiently. For these layouts, the resistors were implemented with high-resistor layer that gives more resistance per squared micron and occupies less space. Good matching techniques and interdigitation, were implemented.

5.2 Recommendations

1. Good performance of a circuit does not depend only on careful
design; it also depends on how you test the circuit. A wrong test may hide the features you are looking for in a new circuit architecture. In my case I ran through several problems, the first one was that I did not put any attention to input common-mode voltage range, so I was pulling some of the transistors out of saturation. The second problem occurred while testing the circuit as a voltage follower, without the using the feedback floating battery like the one used in Figure 5.2, and I had to use a small pulse as the input voltage since a big pulse will take some of the transistors out of saturation. The input pulse was not big enough to force the op-amp to deliver its maximum current. At the end I change the configuration to be a voltage inverter like in Figure 5.2, which allows higher input voltages.

2. The first step in designing an op-amp is to determine the required needed specifications. There are plenty of different parameters that can be tested in a circuit and it is better if you can determine what parameters are of interest and then how to come up with a design that will fulfill the specifications.

3. Before sending layouts to fabrication make sure to simulate every wanted parameter. It is better to have every parameter of interest characterized. Otherwise surprises may strike you at the last moment. As explained in the first recommendation, I decided to change test scheme from a voltage follower to a voltage inverter. However, my chip was already
fabricated and I did not have any internal circuitry that will implement the floating battery [Ram98]. I had to use an external old battery with a voltage close to 0.6V.

4. The best way of proving that our proposed topologies are better than other existing topologies is to design each of them with the same specifications and compare their performances in simulation and testing in lab. I did not layout a circuit such as Full-A or Class A-AB to compare its performance against the Full-AB and Hybrid op-amps.

5. Some sections in my design could have been done trying to lower the static power dissipation. For example the first stages in my op-amps could have been designed for lower bias currents, instead of 100µA I could have chosen 20µA. VCM circuit in Chapter 3 could have been designed with a lower biasing current; the static current flowing through this circuit is 40uA and is quite a lot. The static current required by the VCM circuit could be reduced by a factor of 10 or more.
APPENDICES
A MODEL PARAMETERS AND SPICE LISTINGS

A.1 Model Parameters and SPICE Listings

N-type Metal Oxide Semiconductor (NMOS) and P-type Metal Oxide
Semiconductor (PMOS) models are obtained from MOSIS at this web
address http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-
c5n/t09w-params.txt

A.1.1 NMOS Model

```
.MODEL NMOS NMOS (LEVEL = 49 +VERSION = 3.1
+TNOM = 27 TOX = 1.39E-8 +XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.6788717
+K1 = 0.8593553 K2 = -0.0910679 K3 = 23.3283144 +K3B = -7.595426 W0 = 1E-8
+DVT0W = 0 DVT1W = 0 DVT2W = 0 +DVT0 = 2.4669336 DVT1 = 0.406657 DVT2 = -0.143346
+U0 = 457.0330416 UA = 1.689519E-13 UB = 1.599854E-18 +UC = 1.984294E-11 VSAT = 1.686671E5
+A0 = 0.6203431 +AGS = 0.1442592 B0 = 2.668396E-6 +B1 = 5E-6
+KETA = -3.786955E-3 A1 = 2.884702E-4 +A2 = 0.3452819 +RDSW = 1.363604E3 +PRWG = 0.0409292
+PRWB = 0.0319167 +WR = 1 WINT = 2.515891E-7 +LINT = 2.110296E-8
+XL = 0 XW = 0 DWG = -1.477336E-8 +DWB = 5.582307E-8 VOFF = 0 +NFACTOR = 1.0650616
+CIT = 0 CDSC = 2.4E-4 +CDSCD = 0 +CDSCB = 0 +ETA0 = 0.0101532 +ETAB = -8.714158E-4
+DSUB = 0.1551987 PCLM = 2.530607 +PDIBLC1 = -0.1962599
```
A.1.2 PMOS Model

.MODEL PMOS PMOS ( LEVEL = 49
+VERSION = 3.1      TNOM = 27      TOX = 1.39E-8
+XJ = 1.5E-7      NCH = 1.7E17      VTH0 = -0.898977
+K1 = 0.5461154      K2 = 9.298245E-3      K3 = 7.5117776
+K3B = -0.8279481      W0 = 1.724364E-7      NLX = 8.928853E-8
+DVT0W = 0      DVT1W = 0      DVT2W = 0
+DVT0 = 2.347617      DVT1 = 0.5060168      DVT2 = -0.100407
+U0 = 216.7973058      UA = 2.947145E-9      UB = 1.060583E-21

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+UC = -5.83518E-11 VSAT = 1.774355E5 A0 = 0.8439205
+AGS = 0.1410468 B0 = 9.969117E-7 B1 = 5E-6
+KETA = -2.398617E-3 A1 = 0 A2 = 0.3
+RDSW = 3E3 PRWG = -0.0389571 PRWB = -0.0140735
+WR = 1 WINT = 2.909428E-7 LINT = 4.485568E-8
+XL = 0 XW = 0 DWG = -1.814079E-8
+DWB = 1.981066E-8 VOFF= -0.0755572 NFACTOR= 0.8079503
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 0.0748999 ETAB = -0.0502393
+DSUB = 0.8469718 PCLM = 2.1791259 PDIBLC1 = 0.0643399
+PDIBLC2 = 4.109531E-3 PDIBLCB = -0.0403314
+DROUT=0.2556781
+PSCBE1 = 1.295783E10 PSCBE2 = 1.262428E-9 PVAG = 0
+DELTA = 0.01 RSH = 101.1 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -0.11
+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WL = 0 WLN = 1 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.31E-10 CGSO = 2.31E-10 CGBO = 1E-9
+CJ = 7.241671E-4 PB = 0.9492892 MJ = 0.4954503
+CJSW = 2.700407E-10 PBSW = 0.9896207 MJSW = 0.2960835
+CJSWG = 6.4E-11 PBSWG = 0.9896207MJSWG = 0.2960835
+CF = 0 PVTH0 = 5.98016E-3 PRDSW = 14.8598424
+PK2 = 3.73981E-3 WKETA = 1.1447E-3
+LKETA = -3.606352E-3 )

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A.1.3 Full-AB Op-Amp SPICE Listing (Chapter 3)

* Main circuit: Full-AB

XQCCFB_1 bbatt biasn biasp ida iq vdd vss w z battery_single2
M5 2 2 vss vss NMOS L='4*l' W='307*l' AD='307*l*5*l' PD='2*l*(307+5)'
AS='307*l*5*l' PS='2*l*(307+5)'
M6 z 2 vss vss NMOS L='4*l' W='307*l' AD='307*l*5*l' PD='2*l*(307+5)'
AS='307*l*5*l' PS='2*l*(307+5)'
M7 N43 ibias vss vss NMOS L='4*l' W='80*l' AD='80*l*5*l' PD='2*l*(80+5)'
AS='80*l*5*l' PS='2*l*(80+5)'
M8 ibias ibias vss vss NMOS L='4*l' W='75*l' AD='75*l*5*l' PD='2*l*(75+5)'
AS='75*l*5*l' PS='2*l*(75+5)'
Moutn out z vss vss NMOS L='2*l' W='510*l' AD='510*l*5*l' PD='2*l*(510+5)'
AS='510*l*5*l' PS='2*l*(510+5)'
M4 N43 vcm 1 1 PMOS L='4*l' W='230*l' AD='230*l*5*l' PD='2*l*(230+5)'
AS='230*l*5*l' PS='2*l*(230+5)'
M1 2 v- 1 1 PMOS L='4*l' W='921*l' AD='921*l*5*l' PD='2*l*(921+5)'
AS='921*l*5*l' PS='2*l*(921+5)'
M2 z v+ 1 1 PMOS L='4*l' W='921*l' AD='921*l*5*l' PD='2*l*(921+5)'
AS='921*l*5*l' PS='2*l*(921+5)'
M3 1 N43 vdd vdd PMOS L='4*l' W='2379*l' AD='2379*l*5*l' PD='2*l*(2379+5)'
AS='2379*l*5*l' PS='2*l*(2379+5)'
Moutp out w vdd vdd PMOS L='2*l' W='1535*l' AD='1535*l*5*l' PD='2*l*(1535+5)'
AS='1535*l*5*l' PS='2*l*(1535+5)'
Xvcm_1 ibias2 v- v+ vcm vdd vss vcm

* End of main circuit: Full-AB

.SUBCKT QCCFB bbatt biasn biasp ida lq vdd vss w z
M4b N50 biasn N7 vss NMOS L='4*l' W='31*l' AD='31*l*5*l' PD='2*l*(31+5)'
AS='31*l*5*l' PS='2*l*(31+5)'
M2b N7 lq vss vss NMOS L='4*l' W='31*l' AD='31*l*5*l' PD='2*l*(31+5)'
AS='31*l*5*l' PS='2*l*(31+5)'
M1b lq lq vss vss NMOS L='4*l' W='31*l' AD='31*l*5*l' PD='2*l*(31+5)'

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AS='31*l*5*l' PS='2*l*(31+5)'
M3b mx lg vss vss NMOS L='4*l' W='31*l' AD='31*l*5*l' PD='2*l*(31+5)'
AS='31*l*5*l' PS='2*l*(31+5)'
M2da N19 ida vss vss NMOS L='6*l' W='52*l' AD='52*l*5*l' PD='2*l*(52+5)' AS='52*l*5*l' PS='2*l*(52+5)'
M1da ida ida vss vss NMOS L='6*l' W='52*l' AD='52*l*5*l' PD='2*l*(52+5)' AS='52*l*5*l' PS='2*l*(52+5)'
M1 y y vss vss NMOS L='2*l' W='51*l' AD='51*l*5*l' PD='2*l*(51+5)'
AS='51*l*5*l' PS='2*l*(51+5)'
M3da N86 ida vss vss NMOS L='6*l' W='52*l' AD='52*l*5*l' PD='2*l*(52+5)' AS='52*l*5*l' PS='2*l*(52+5)'
M6 x N47 vss vss NMOS L='6*l' W='83*l' AD='83*l*5*l' PD='2*l*(83+5)'
AS='83*l*5*l' PS='2*l*(83+5)'
M11 w N47 vss vss NMOS L='6*l' W='83*l' AD='83*l*5*l' PD='2*l*(83+5)' AS='83*l*5*l' PS='2*l*(83+5)'
M7 N45 N47 vss vss NMOS L='6*l' W='83*l' AD='83*l*5*l' PD='2*l*(83+5)' AS='83*l*5*l' PS='2*l*(83+5)'
M8 N47 bbatt N45 vss NMOS L='6*l' W='83*l' AD='83*l*5*l' PD='2*l*(83+6)' AS='83*l*5*l' PS='2*l*(83+6)'
M6b N51 N50 vdd vdd PMOS L='4*l' W='93*l' AD='93*l*5*l' PD='2*l*(93+5)' AS='93*l*5*l' PS='2*l*(93+5)'
M5b N50 biasp N51 vdd vss PMOS L='4*l' W='93*l' AD='93*l*5*l' PD='2*l*(93+5)' AS='93*l*5*l' PS='2*l*(93+5)'
M7b y N50 vdd vdd PMOS L='4*l' W='93*l' AD='93*l*5*l' PD='2*l*(93+5)' AS='93*l*5*l' PS='2*l*(93+5)'
M3 vss mx N64 N64 PMOS L='6*l' W='1244*l' AD='1244*l*5*l' PD='2*l*(1244+5)' AS='1244*l*5*l' PS='2*l*(1244+5)'
M4 N86 x N64 N64 PMOS L='6*l' W='1244*l' AD='1244*l*5*l' PD='2*l*(1244+5)' AS='1244*l*5*l' PS='2*l*(1244+5)'
M4da N19 N19 vdd vdd PMOS L='6*l' W='750*l' AD='750*l*5*l' PD='2*l*(750+5)' AS='750*l*5*l' PS='2*l*(750+5)'
M5da N64 N19 vdd vdd PMOS L='6*l' W='1500*l' AD='1500*l*5*l' PD='2*l*(1500+5)' AS='1500*l*5*l' PS='2*l*(1500+5)'
M2 mx mx vdd vdd PMOS L='2*l' W='153*l' AD='153*l*5*l' PD='2*l*(153+5)' AS='153*l*5*l' PS='2*l*(153+5)'

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M5 y N86 vdd vdd PMOS L='6*I' W='249*I' AD='249*I*5*I'
P'D='2*I*(249+5)' AS='249*I*5*I' PS='2*I*(249+5)'
M10 z N86 vdd vdd PMOS L='6*I' W='249*I' AD='249*I*5*I'
P'D='2*I*(249+5)' AS='249*I*5*I' PS='2*I*(249+5)'
M9 N47 N86 vdd vdd PMOS L='6*I' W='249*I' AD='249*I*5*I'
P'D='2*I*(249+5)' AS='249*I*5*I' PS='2*I*(249+5)'
R1 y x 30k TC=0.0, 0.0
R2 z w 30k TC=0.0, 0.0
.ENDS

.SUBCKT vcm ibias v1 v2 vcm vdd vss
M8 N3 ibias vss vss NMOS L='4*I' W='108*I' AD='108*I*5*I'
M9 vcm ibias vss vss NMOS L='4*I' W='108*I' AD='108*I*5*I'
M10 ibias ibias vss vss NMOS L='4*I' W='108*I' AD='108*I*5*I'
M1 vss v1 N24 N24 PMOS L='4*I' W='103*I' AD='103*I*5*I'
P'D='2*I*(103+5)' AS='103*I*5*I' PS='2*I*(103+5)'
M3 vcm vcm N28 N28 PMOS L='4*I' W='103*I' AD='103*I*5*I'
P'D='2*I*(103+5)' AS='103*I*5*I' PS='2*I*(103+5)'
M2 vcm vcm N24 N24 PMOS L='4*I' W='103*I' AD='103*I*5*I'
P'D='2*I*(103+5)' AS='103*I*5*I' PS='2*I*(103+5)'
M4 vss v2 N28 N28 PMOS L='4*I' W='103*I' AD='103*I*5*I'
P'D='2*I*(103+5)' AS='103*I*5*I' PS='2*I*(103+5)'
M5 N24 N3 vdd vdd PMOS L='4*I' W='207*I' AD='207*I*5*I'
P'D='2*I*(207+5)' AS='207*I*5*I' PS='2*I*(207+5)'
M6 N28 N3 vdd vdd PMOS L='4*I' W='207*I' AD='207*I*5*I'
P'D='2*I*(207+5)' AS='207*I*5*I' PS='2*I*(207+5)'
M7 N3 N3 vdd vdd PMOS L='4*I' W='207*I' AD='207*I*5*I'
P'D='2*I*(207+5)' AS='207*I*5*I' PS='2*I*(207+5)'
.ENDS

* Lambda (l) is 0.3 microns
.param I=0.3u

* Input circuit file
.include C:\My_Documents\VLSI\ABopamp3\tspice\fabout4.sp
*include Z:\VLSI\ABopamp3\tspice\fabout2.sp
* SPICE models
.include C:\My_Documents\VLSI\ABopamp3\tspice\t16w05n.md
*include Z:\VLSI\ABopamp3\tspice\t16w05n.md
.include C:\My_Documents\VLSI\ABopamp3\tspice\t16w05p.md
*include Z:\VLSI\ABopamp3\tspice\t16w05p.md

* Important (Default) Simulation Options
* .options abstol=5e-010 chargetol=1e-014 gmin=0 moscap=0
* .options relchargetol=reltol reltol=1e-4 vntol=1e-3
.options abstol=1e-012 chargetol=1e-015 gmin=1e-15 moscap=1
.options relchargetol=1e-6 reltol=1e-6 vntol=1e-6

* Grid Size and Range for MOS I-V Internal Tables
* To turn off internal tables, set deftables to 0
.options deftables=0
.vrange mos 5.5
.gridsize mos 128 256 64

* DC Power Supplies
VVdd Vdd Gnd 1.5
VVss Vss Gnd 0

* DC Inputs
*v1 v+ gnd 1.5319e-001 AC 1 0
*v2 v- gnd 0.15
*v2 v- v+ 0
*Differential input signals
*v1 vv1 gnd 0
*v2 vcm gnd 0.15
*e1 v+ vcm vv1 gnd 1
*e1 v- vcm gnd vv1 1
I1 vdd ibias 25u
I2 vdd ibias2 10u
*DC inputs for floating battery
I3 vdd iq 20u
I4 vdd ida 5u
v3 vdd biasp 1.3
v4 biasn vss 1.2
v5 bbatt vss 1.43

*DC sweep analysis settings to measure transconductance characteristic
*R1 out tp 100
*v3t tp gnd 0.75

*AC analysis settings
*R1 out va- 100Meg
*v7 va- v- 0.6
*C1 v- gnd 10u

*Transient Analysis - voltage follower
*Vvin v+ gnd pulse(0.1 0.3 2n 1n 1n 30.25n 62.5n)
*Vvin v+ gnd 0.1 pulse(0.1 0.3 2n 1n 1n 49n 100n)
*Vvin v+ gnd pulse(0.1 0.3 2n 1n 1n 99n 200n)
*Vvin v+ gnd 0.15 pulse(0 0.3 2n 2n 2n 173n 350n)
*Vvin v+ gnd pulse(0 0.3 5n 10n 10n 490n 1000n)
*v7 out v- 0.6

*Transient Analysis - inverter
R1i out vb- 300k
C1i out vb- 0.5p
v1i vb- v- 0.6
R2i vin vb- 300k
C2i vin vb- 0.5p
Vvin vin gnd 0.75 pulse(0 1.5 10n 10n 490n 1000n)
*Vvin vin gnd 1.5 pulse(0 1.5 2n 1n 1n 49n 100n)
*Vvin vin gnd 0.75 pulse(0 1.5 2n 1n 1n 99n 200n)
*Vvin vin gnd pulse(0 1.5 2n 2n 173n 350n)
*VVvin vin GND SIN (0.75 0.2 2.8Meg)
*Vvin vin gnd pulse(0 2 2n 5n 5n 195n 400n)
v2i v+ gnd 0.15

*Loads
Cload out gnd 20p
Cc z tp1 4.4p
Rz tp1 out 1.5k
Cc2 z w 2p

*Measurements
.measure dc voffset1 find v(v+) when v(out)=0.75 cross=1
.measure dc offset param='voffset1-0.15'
.measure dc Itotal find l(Vvss) when V(out)=0.75 cross=1
.measure dc Spower param='1.5*Itotal'
.measure dc x1 when v(out)=1 cross=1
.measure dc x2 when v(out)=0.5 cross=1
.measure dc Aol param='0.5/(x1-x2)'
.measure dc AoldB param='20*log10(Aol)'

*AC measurements
.measure ac p180 find Vp(Out) when Vdb(Out)=0 cross=1
.measure ac PM param='180-abs(p180)'
.measure ac GM find Vdb(Out) when vp(Out)=-178 cross=1
.measure ac AoldB find Vdb(Out) at=50
.measure ac Aol param='10^(AoldB/20)'
.measure ac ft when Vdb(Out)=0 cross=1

*Tran measurements
.measure tran x1 when v(out)=1 cross=1
.measure tran x2 when v(out)=.5 cross=1
.measure tran SRd param='0.5/(x2-x1)'
.measure tran x3 when v(out)=1 cross=2
.measure tran x4 when v(out)=.5 cross=2
.measure tran SRu param='0.5/(x3-x4)'

*Tran measurements - Voltage follower-
.measure tran x1f when v(out)=0.8 cross=1
.measure tran x2f when v(out)=0.7 cross=1
.measure tran SRdf param='abs(0.1/(x2f-x1f))'
.measure tran x3f when v(out)=0.8 cross=2
.measure tran x4f when v(out)=0.7 cross=2
.measure tran SRuf param='abs(0.1/(x3f-x4f))'

*Analysis
.op
*.dc lin v1 0.151 0.155 0.00001
*.dc lin v1 0 0.3 0.00001
*.dc lin v1 0.146 0.16 0.00001
*.dc lin l3 5u 12u 0.1u
A.1.4 Full-AB Op-Amp SPICE Listing (Chapter 4)

* Main circuit: Full-AB, Chapter 4.

XQCCFB_1 ibias2 ibias3 Iqo vbias vdd vss x y Battery

M5 N4 N4 vss vss NMOS L='4*I' W='2672*I' AD='2672*5*I' I'
PD='2*I'(2672+5) AS='2672*5*I' PS='2*I'(2672+5)'

M8 ibias ibias vss vss NMOS L='4*I' W='134*I' AD='134*5*I' I'
PD='2*I'(134+5) AS='134*5*I' PS='2*I'(134+5)'

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Moutn out y vss vss NMOS L='7*I' W='1336*I' AD='1336*5*I*I' PD='2*I*(1336+5)' AS='1336*5*I*I' PS='2*I*(1336+5)'


M2 x v+ low vdd PMOS L='4*I' W='1336*I' AD='1336*5*I*I' PD='2*I*(1336+5)' AS='1336*5*I*I' PS='2*I*(1336+5)'

M3 low N2 vdd vdd PMOS L='4*I' W='1336*I' AD='1336*5*I*I' PD='2*I*(1336+5)' AS='1336*5*I*I' PS='2*I*(1336+5)'

M4 N2 N1 low vdd PMOS L='4*I' W='1336*I' AD='1336*5*I*I' PD='2*I*(1336+5)' AS='1336*5*I*I' PS='2*I*(1336+5)'


M1 N4 v- low vdd PMOS L='4*I' W='1336*I' AD='1336*5*I*I' PD='2*I*(1336+5)' AS='1336*5*I*I' PS='2*I*(1336+5)'

Xvcm_module_1 ibias4 ibias5 ibias6 N1 v+ v- vdd vss vcm_module

* End of main circuit: Full-AB, Chapter 4

.SUBCKT QCCFB ibias1 ibias2 lqo vbias vdd vss X Y


M10 xp N7 vss vss NMOS L='7*I' W='7*I' AD='7*5*I' PD='2*I*(7+5)' AS='7*I*5*I' PS='2*I*(7+5)'

M12 N4 N7 vss vss NMOS L='7*I' W='7*I' AD='7*I*5*I' PD='2*I*(7+5)' AS='7*I*5*I' PS='2*I*(7+5)'

M15 N7 vbias N4 vss vss NMOS L='7*I' W='7*I' AD='7*I*5*I' PD='2*I*(7+5)' AS='7*I*5*I' PS='2*I*(7+5)'

M14 X N7 vss vss NMOS L='7*I' W='7*I' AD='7*I*5*I' PD='2*I*(7+5)' AS='7*I*5*I' PS='2*I*(7+5)'


M1 yp yp vss vss NMOS L='7*I' W='14*I' AD='14*5*I*I' PD='2*I*(14+5)'

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AS='14*5*l*l' PS='2*l*(14+5)'
   M9 yp N6 vdd vdd PMOS L='7*l' W='10*l' AD='10*l*5*l' PD='2*l*(10+5)'
   AS='10*l*5*l' PS='2*l*(10+5)'
   M11 N7 N6 vdd vdd PMOS L='7*l' W='10*l' AD='10*l*5*l' PD='2*l*(10+5)'
   AS='10*l*5*l' PS='2*l*(10+5)'
   M13 Y N6 vdd vdd PMOS L='7*l' W='10*l' AD='10*l*5*l' PD='2*l*(10+5)'
   AS='10*l*5*l' PS='2*l*(10+5)'
   M4 N6 xp N3 N3 PMOS L='4*l' W='200*l' AD='200*l*5*l' PD='2*l*(200+5)' AS='200*l*5*l' PS='2*l*(200+5)'
   M5 N3 ibias1 vdd vdd PMOS L='4*l' W='200*l' AD='200*l*5*l' PD='2*l*(200+5)' AS='200*l*5*l' PS='2*l*(200+5)'
   M6 ibias1 ibias1 vdd vdd PMOS L='4*l' W='200*l' AD='200*l*5*l' PD='2*l*(200+5)' AS='200*l*5*l' PS='2*l*(200+5)'
   M2 mx mx vdd vdd PMOS L='7*l' W='20*l' AD='20*l*5*l' PD='2*l*(20+5)' AS='20*l*5*l' PS='2*l*(20+5)'
   R1 yp xp 150k TC=0.0, 0.0
   R2 Y X 150k TC=0.0, 0.0
   R3 Iqo vss 1 TC=0.0, 0.0
   g4 vdd yp Iqo vss 1
   g5 mx vss Iqo vss 1
   .ENDS

   .SUBCKT vcm_module ibias1 ibias2 ibias3 out v+ v- vdd vss
   M5 out ibias3 vss vss NMOS L='5*l' W='200*l' AD='200*l*5*l' PD='2*l*(200+5)' AS='200*l*5*l' PS='2*l*(200+5)'
   M6 ibias3 ibias3 vss vss NMOS L='5*l' W='200*l' AD='200*l*5*l' PD='2*l*(200+5)' AS='200*l*5*l' PS='2*l*(200+5)'
   M7 ibias1 ibias1 vdd vdd PMOS L='5*l' W='134*l' AD='134*l*5*l' PD='2*l*(134+5)' AS='134*l*5*l' PS='2*l*(134+5)'
   M9 biasp2 ibias2 vdd vdd PMOS L='5*l' W='134*l' AD='134*l*5*l' PD='2*l*(134+5)' AS='134*l*5*l' PS='2*l*(134+5)'
   M8 biasp1 ibias1 vdd vdd PMOS L='5*l' W='134*l' AD='134*l*5*l' PD='2*l*(134+5)' AS='134*l*5*l' PS='2*l*(134+5)'
   M10 ibias2 ibias2 vdd vdd PMOS L='5*l' W='134*l' AD='134*l*5*l'
PD='2*l(134+5)‘ AS='134*l*5*l’ PS='2*l(134+5)‘

M1 vss v- biasp1 vdd PMOS L='5*l‘ W='134*l‘ AD='134*l*5*l‘
PD='2*l(134+5)‘ AS='134*l*5*l‘ PS='2*l(134+5)‘

M3 out out biasp2 vdd PMOS L='5*l‘ W='134*l‘ AD='134*l*5*l‘
PD='2*l(134+5)‘ AS='134*l*5*l‘ PS='2*l(134+5)‘

M2 out out biasp1 vdd PMOS L='5*l‘ W='134*l‘ AD='134*l*5*l‘
PD='2*l(134+5)‘ AS='134*l*5*l‘ PS='2*l(134+5)‘

M4 vss v+ biasp2 vdd PMOS L='5*l‘ W='134*l‘ AD='134*l*5*l‘
PD='2*l(134+5)‘ AS='134*l*5*l‘ PS='2*l(134+5)‘

.ENDS

* Lambda (l) is 0.3 microns
.param l=0.3u

* Input circuit file
*.include C:\My_Documents\VLSI\ABopamp\Schematic\abopamp2\tesis_rev2\tspice\2stageopamp.sp
.include C:\My_Documents\VLSI\tesis_rev2\tspice\2stageopamp.sp
* SPICE models
*.include C:\My_Documents\VLSI\tesis_rev2\tspice\cmost.txt
*.include C:\My_Documents\VLSI\tesis_rev2\tspice\t16w05n.md
*.include C:\My_Documents\VLSI\tesis_rev2\tspice\t16w05p.md
.include C:\My_Documents\VLSI\ABopamp\Layout\t13r05n.md
.include C:\My_Documents\VLSI\ABopamp\Layout\t13r05p.md

* Important (Default) Simulation Options
* .options abstol=5e-010 chargetol=1e-014 gmin=0 moscap=0
* .options relchargetol=reltol reltol=1e-4 vntol=1e-3
.options abstol=1e-012 chargetol=1e-015 gmin=1e-15 moscap=1
.options relchargetol=1e-6 reltol=1e-6 vntol=1e-6
* Grid Size and Range for MOS I-V Internal Tables
* To turn off internal tables, set deftables to 0
  .options deftables=0
  .vrange mos 5.5
  .gridsize mos 128 256 64

* DC Power Supplies
  VVdd Vdd Gnd 1.5
  VVss Vss Gnd 0

* DC Inputs
  v1 v+ gnd 1.4908e-001 AC 1 0
  *v2 v- gnd 0.15
  I1 vdd ibias 15u

*DC inputs for floating battery
  I3 vdd iqo 2u
  I4 vdd ibias3 2u
  I5 ibias2 vss 4u
  v5 vbias vss 1.3

*DC inputs for vcm
  I6 ibias4 vss 4u
  I7 ibias5 vss 4u
  I8 vdd ibias6 4u

*DC sweep analysis settings to measure transconductance characteristic
  *R1 out tp 100
  *v3t tp gnd 0.75
*AC analysis settings
R1 out va- 100Meg
v7 va- v- 0.6
C1 v- gnd 10u

*Transient Analysis - voltage follower
*Vvin v+ gnd pulse(0.1 0.3 5n 10n 10n 490n 1000n)
*Vvin v+ gnd pulse(0.1 0.3 5n 0.1u 0.1u 2.4u 5u)
*Vvin v+ gnd pulse(0.1 0.3 5n 0.1u 0.1u 4.9u 10u)
*Vvin v+ gnd pulse(0.1 0.3 5n 0.1u 0.1u 49.9u 100u)
*VVvin v+ GND SIN (0.15 100m 3.5meg)
*v7 v- out 0

*Transient Analysis - voltage follower
*R1i out vb- 100k
*C1i out vb- 0.1p
*v1i vb- v- 0.6
*R2i vin vb- 100k
*C2i vin vb- 0.1p
*Vvin vin gnd pulse(0 1.5 5n 0.01u 0.01u 2.49u 5u)
*Vvin vin gnd pulse(0 1.5 5n 0.1u 0.1u 4.9u 10u)
*Vvin vin gnd pulse(0 1.5 5n 0.1u 0.1u 49.9u 100u)
*v2i v+ gnd 0.15

*Loads
Cload out gnd 20p
Rload out gnd 10Meg
Cc x tp1 20p
Rz tp1 out 1k
*Cc2 z w 1p
*.param C=1k

*Measurements
.measure dc voffset1 find v(v+) when v(out)=0.75 cross=1
.measure dc offset param='voffset1-0.15'
.measure dc Itotal find I(Vvss) when V(out)=0.75 cross=1
.measure dc Spower param='1.5*Itotal'
.measure dc x1 when v(out)=1 cross=1
.measure dc x2 when v(out)=0.5 cross=1
.measure dc Aol param='0.5/(x1-x2)'
*.measure dc AoldB param='20*log10(Aol)'

*AC measurements
.measure ac p180 find Vp(Out) when Vdb(Out)=0 cross=1
.measure ac PM param='180-abs(p180)'
.measure ac GM find Vdb(Out) when vp(Out)=-178 cross=1
.measure ac AoldB find Vdb(Out) at=50
.measure ac Aol param='10^(AoldB/20)'
.measure ac ft when Vdb(Out)=0 cross=1

*Tran measurements
.measure tran x1 when v(out)=.250 cross=1
.measure tran x2 when v(out)=.150 cross=1
.measure tran SRu param='0.1/(x2-x1)'
.measure tran x3 when v(out)=.250 cross=2
.measure tran x4 when v(out)=.150 cross=2
.measure tran SRd param='0.1/(x3-x4)'

* Input Waveforms

*Analysis
.op
*.dc lin v1 148.5m 149.5m 10u
*.dc lin v1 140m 160m 10u
*V vin vin gnd 0
*.dc lin Vvin 0 1.5 5.88m
*.dc lin v1 -0.3 0.6 0.0001
*.dc lin v1 0 0.3 0.0001
*.dc lin v1 0 1.5 0.0001
.ac dec 202 10 10G
*.tran/op 0.5u 10u method=bdf
*.tran/op 1n 5u method=bdf
*.tran/op 1n 1u method=bdf
*sweep lin param C 4p 5p 0.1p
*.options prtdel=1.98e-8
*.tran/op 5n 125n method=bdf

* Print Results
*.print dc v(out)
*.print dc is(Moutp) id(Moutn)
*.print dc is(M6) id(M7) i(R1)
*.print dc is(M1) v(1,2)
.print ac vdb(out) vp(out)
*.print tran v(out) v(v+) i(Cc) i(Cload)
*.print tran is(M1) is(M2) id(M5) id(M6)
*.print tran v(z)
*.print tran v(out) v(vin)
*i(Cc) i(Cload)
*.print tran v(v+) v(out)
A.1.5 Class A-AB Op-Amp SPICE Listing

* Main circuit: Class A-AB

XQCCFB_1 bbatt biasn biasp ida iq vdd vss w z battery_single2

M5 2 2 vss vss NMOS L='4*l' W='307*l' AD='307*l*5*l' PD='2*l*(307+5)'
AS='307*l*5*l' PS='2*l*(307+5)'

M6 z 2 vss vss NMOS L='4*l' W='307*l' AD='307*l*5*l' PD='2*l*(307+5)'
AS='307*l*5*l' PS='2*l*(307+5)'

M7 N13 ibias vss vss NMOS L='4*l' W='300*l' AD='300*l*5*l'
PD='2*l*(300+5)' AS='300*l*5*l' PS='2*l*(300+5)'

M8 ibias ibias vss vss NMOS L='4*l' W='75*l' AD='75*l*5*l'
PD='2*l*(75+5)' AS='75*l*5*l' PS='2*l*(75+5)'

Moutn out z vss vss NMOS L='2*l' W='510*l' AD='510*l*5*l'
PD='2*l*(510+6)' AS='510*l*5*l' PS='2*l*(510+6)'

M4 N13 N13 vdd vdd PMOS L='4*l' W='921*l' AD='921*l*5*l'
PD='2*l*(921+5)' AS='921*l*5*l' PS='2*l*(921+5)'

M1 2 v- 1 1 PMOS L='4*l' W='921*l' AD='921*l*5*l' PD='2*l*(921+5)'
AS='921*l*5*l' PS='2*l*(921+5)'

M2 z v+ 1 1 PMOS L='4*l' W='921*l' AD='921*l*5*l' PD='2*l*(921+5)'
AS='921*l*5*l' PS='2*l*(921+5)'

M3 1 N13 vdd vdd PMOS L='4*l' W='1842*l' AD='1842*l*5*l'
PD='2*l*(1842+5)' AS='1842*l*5*l' PS='2*l*(1842+5)'

Moutp out w vdd vdd PMOS L='2*l' W='1535*l' AD='1535*l*5*l'
PD='2*l*(1535+5)' AS='1535*l*5*l' PS='2*l*(1535+5)'

* End of main circuit: Class A-AB

.SUBCKT QCCFB bbatt biasn biasp ida lq vdd vss w z

M4b N50 biasn N7 vss NMOS L='4*l' W='154*l' AD='154*l*5*l'
PD='2*l*(154+5)' AS='154*l*5*l' PS='2*l*(154+5)'

M2b N7 lq vss vss NMOS L='4*l' W='154*l' AD='154*l*5*l'
PD='2*l*(154+5)' AS='154*l*5*l' PS='2*l*(154+5)'

M1b lq lq vss vss NMOS L='4*l' W='154*l' AD='154*l*5*l'

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PD='2*l'(154+5) AS='154*l*5*l' PS='2*l'(154+5)

M3b mx lq vss vss NMOS L='4*l' W='154*l' AD='154*l*5*l'
PD='2*l'(154+5) AS='154*l*5*l' PS='2*l'(154+5)

M2da N19 ida vss vss NMOS L='6*l' W='52*l' AD='52*l*5*l'
PD='2*l'(52+5) AS='52*l*5*l' PS='2*l'(52+5)

M1da ida ida vss vss NMOS L='6*l' W='52*l' AD='52*l*5*l'
PD='2*l'(52+5) AS='52*l*5*l' PS='2*l'(52+5)

M1 y y vss vss NMOS L='2*l' W='51*l' AD='51*l*5*l' PD='2*l'(51+5)
AS='51*l*5*l' PS='2*l'(51+5)

M3da N86 ida vss vss NMOS L='6*l' W='52*l' AD='52*l*5*l'
PD='2*l'(52+5) AS='52*l*5*l' PS='2*l'(52+5)

M6 x N47 vss vss NMOS L='6*l' W='83*l' AD='83*l*5*l' PD='2*l'(83+5)
AS='83*l*5*l' PS='2*l'(83+5)

M11 w N47 vss vss NMOS L='6*l' W='83*l' AD='83*l*5*l'
PD='2*l'(83+5) AS='83*l*5*l' PS='2*l'(83+5)

M7 N45 N47 vss vss NMOS L='6*l' W='83*l' AD='83*l*5*l'
PD='2*l'(83+5) AS='83*l*5*l' PS='2*l'(83+5)

M8 N47 bbatt N45 vss vss NMOS L='6*l' W='83*l' AD='83*l*5*l'
PD='2*l'(83+6) AS='83*l*5*l' PS='2*l'(83+6)

M6b N51 N50 vdd vdd PMOS L='4*l' W='462*l' AD='462*l*5*l'
PD='2*l'(462+5) AS='462*l*5*l' PS='2*l'(462+5)

M5b N50 biasp N51 vdd vdd PMOS L='4*l' W='462*l' AD='462*l*5*l'
PD='2*l'(462+5) AS='462*l*5*l' PS='2*l'(462+5)

M7b y N50 vdd vdd PMOS L='4*l' W='462*l' AD='462*l*5*l'
PD='2*l'(462+5) AS='462*l*5*l' PS='2*l'(462+5)

M3 vss mx N64 N64 PMOS L='6*l' W='1244*l' AD='1244*l*5*l'
PD='2*l'(1244+5) AS='1244*l*5*l' PS='2*l'(1244+5)

M4 N86 x N64 N64 PMOS L='6*l' W='1244*l' AD='1244*l*5*l'
PD='2*l'(1244+5) AS='1244*l*5*l' PS='2*l'(1244+5)

M4da N19 N19 vdd vdd PMOS L='6*l' W='750*l' AD='750*l*5*l'
PD='2*l'(750+5) AS='750*l*5*l' PS='2*l'(750+5)

M5da N64 N19 vdd vdd PMOS L='6*l' W='1500*l' AD='1500*l*5*l'
PD='2*l'(1500+5) AS='1500*l*5*l' PS='2*l'(1500+5)

M2 mx mx vdd vdd PMOS L='2*l' W='153*l' AD='153*l*5*l'
PD='2*l'(153+5) AS='153*l*5*l' PS='2*l'(153+5)
M5 y N86 vdd vdd PMOS L='6*l' W='249*l' AD='249*l*5*l' PD='2*l*(249+5)' AS='249*l*5*l' PS='2*l*(249+5)'
M10 z N86 vdd vdd PMOS L='6*l' W='249*l' AD='249*l*5*l' PD='2*l*(249+5)' AS='249*l*5*l' PS='2*l*(249+5)'
M9 N47 N86 vdd vdd PMOS L='6*l' W='249*l' AD='249*l*5*l' PD='2*l*(249+5)' AS='249*l*5*l' PS='2*l*(249+5)'
   R1 y x 30k TC=0.0, 0.0
   R2 z w 30k TC=0.0, 0.0
   .ENDS

* Lambda (l) is 0.3 microns
   .param l=0.3u

* Input circuit file
   .include C:\My_Documents\VLSI\ABopamp3\tspice\sabout4.sp
   *.include Z:\VLSI\ABopamp3\tspice\sabout2.sp
* SPICE models
   .include C:\My_Documents\VLSI\ABopamp3\tspice\t16w05n.md
   *.include Z:\VLSI\ABopamp3\tspice\t16w05n.md
   .include C:\My_Documents\VLSI\ABopamp3\tspice\t16w05p.md
   *.include Z:\VLSI\ABopamp3\tspice\t16w05p.md

* Important (Default) Simulation Options
* .options abstol=5e-010 chargetol=1e-014 gmin=0 moscap=0
* .options relchargetol=reltol reltol=1e-4 vntol=1e-3
   .options abstol=1e-012 chargetol=1e-015 gmin=1e-15 moscap=1
   .options relchargetol=1e-6 reltol=1e-6 vntol=1e-6

* Grid Size and Range for MOS I-V Internal Tables
* To turn off internal tables, set deftables to 0
   .options deftables=0

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.vrange mos 5.5
.gridsize mos 128 256 64

* DC Power Supplies
VVdd Vdd Gnd 1.5
VVss Vss Gnd 0

* DC Inputs
*v1 v+ gnd 1.5321e-001 AC 1 0
*v2 v- gnd 0.15
*v2 v- v+ 0

* Differential input signals
*v1 vv1 gnd 0
*v2 vcm gnd 0.15
*e1 v+ vcm vv1 gnd 1
*e1 v- vcm gnd vv1 1
I1 vdd ibias 25u

* DC inputs for floating battery
I3 vdd iq 7u
I4 vdd ida 5u
v3 vdd biasp 1.3
v4 biasn vss 1.2
v5 bbatt vss 1.43

* DC sweep analysis settings to measure transconductance characteristic
*R1 out tp 100
*v3t tp gnd 0.75
*AC analysis settings
*R1 out va- 100Meg
*v7 va- v- 0.6
*C1 v- gnd 10u

*Transient Analysis - voltage follower
*Vvin v+ gnd pulse(0.1 0.3 2n 1n 1n 30.25n 62.5n)
*Vvin v+ gnd 0.1 pulse(0.1 0.3 2n 1n 1n 49n 100n)
*Vvin v+ gnd pulse(0.1 0.3 2n 1n 1n 99n 200n)
*Vvin v+ gnd pulse(0 0.3 2n 2n 2n 173n 350n)
*Vvin v+ gnd pulse(0.1 0.4 5n 10n 10n 490n 1000n)
*v7 out v- 0.6

*Transient Analysis - inverter
R1i out vb- 300K
C1i out vb- 0.5p
v1i vb- v- 0.6
R2i vin vb- 300k
C2i vin vb- 0.5p
Vvin vin gnd 0.75 pulse(0 1.5 5n 10n 10n 490n 1000n)
*Vvin vin gnd 1.5 pulse(0 1.5 2n 1n 1n 49n 100n)
*Vvin vin gnd 0.75 pulse(0 1.5 2n 2n 2n 173n 350n)
*Vvin vin gnd pulse(0 1.5 2n 1n 1n 99n 200n)
*Vvin vin gnd pulse(0 2 2n 5n 5n 195n 400n)
v2i v+ gnd 0.15

*Loads
Cload out gnd 20p
Cc z tp1 4.4p
Rz tp1 out 1.5k
Cc2 z w 2p
*.param C=1k

*Measurements
.measure dc voffset1 find v(v+) when v(out)=0.75 cross=1
.measure dc offset param='voffset1-0.15'
.measure dc Itotal find I(Vvss) when V(out)=0.75 cross=1
.measure dc Spower param='1.5*Itotal'
.measure dc x1 when v(out)=1 cross=1
.measure dc x2 when v(out)=0.5 cross=1
.measure dc AOL param='0.5/(x1-x2)'
.measure dc AoldB param='20*log10(Aol)'

*AC measurements
.measure ac p180 find Vp(Out) when Vdb(Out)=0 cross=1
.measure ac PM param='180-abs(p180)'
.measure ac GM find Vdb(Out) when vp(Out)=-178 cross=1
.measure ac AoldB find Vdb(Out) at=50
.measure ac AOL param='10^(AoldB/20)'
.measure ac ft when Vdb(Out)=0 cross=1

*Tran measurements
.measure tran x1 when v(out)=1 cross=1
.measure tran x2 when v(out)=.5 cross=1
.measure tran SRu param='0.5/(x2-x1)'
.measure tran x3 when v(out)=1 cross=2
.measure tran x4 when v(out)=.5 cross=2
.measure tran SRd param='0.5/(x3-x4)'

*Tran measurements - Voltage follower-
.measure tran x1f when v(out)=0.8 cross=1
.measure tran x2f when v(out)=0.7 cross=1
.measure tran SRdf param='abs(0.1/(x2f-x1f))'
.measure tran x3f when v(out)=0.8 cross=2
.measure tran x4f when v(out)=0.7 cross=2
.measure tran SRuf param='abs(0.1/(x3f-x4f))'

* Input Waveforms

* Analysis
    .op
    *dc lin v1 0.15 0.155 0.00001
    *dc lin v1 -0.3 0.6 0.0001
    *dc lin v1 0 0.3 0.0001
    *dc lin v1 0 1.5 0.0001
    *ac dec 202 10 10G
    .tran/op 5n 2u method=bdf
    *tran/op 5n 700n method=bdf
    *sweep lin param C 4p 5p 0.1p

* Print Results
    *.print dc v(out)
    *.print dc is(Moutp) id(Moutn)
    *.print dc is(M6) id(M7) i(R1)
    *.print dc is(M1) v(1,2)
    *.print ac vdb(out) vp(out)
    .print tran  v(out) v(vin) is(Moutp) id(Moutn) i(Cc) i(Cload)
    *.print tran  v(out) v(vin) i(Cc) i(Cload)
    *.print tran  v(out) v(z) v(2) v(v-)
    *.print tran  v(out) v(vin) v(z) v(2) is(m1) is(m2)
    *.print tran  v(out) v(vin) v(1,v-) v(1,v+) i(Cc)

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A.1.6 Full-A Op-Amp SPICE Listing

* Main circuit: Full-A

M4 2 2 vss vss NMOS L='4*l' W='307*l' AD='307*l*5*l' PD='2*l*(307+6)'
AS='307*l*5*l' PS='2*l*(307+6)'
M5 x 2 vss vss NMOS L='4*l' W='307*l' AD='307*l*5*l' PD='2*l*(307+5)'
AS='307*l*5*l' PS='2*l*(307+5)'
M7 out x vss vss NMOS L='2*l' W='307*l' AD='307*l*5*l' PD='2*l*(307+5)'
AS='307*l*5*l' PS='2*l*(307+5)'
M6 out ibias vdd vdd PMOS L='4*l' W='1842*l' AD='1842*l*5*l' PD='2*l*(1842+5)'
AS='1842*l*5*l' PS='2*l*(1842+5)'
M1 2 v- 1 1 PMOS L='4*l' W='921*l' AD='921*l*5*l' PD='2*l*(921+5)'
AS='921*l*5*l' PS='2*l*(921+5)'
M2 x v+ 1 1 PMOS L='4*l' W='921*l' AD='921*l*5*l' PD='2*l*(921+5)'
AS='921*l*5*l' PS='2*l*(921+5)'
M3 1 ibias vdd vdd PMOS L='4*l' W='1842*l' AD='1842*l*5*l' PD='2*l*(1842+5)'
AS='1842*l*5*l' PS='2*l*(1842+5)'
M8 ibias ibias vdd vdd PMOS L='4*l' W='921*l' AD='921*l*5*l' PD='2*l*(921+5)'
AS='921*l*5*l' PS='2*l*(921+5)'

* End of main circuit: Full-A

* Lambda (l) is 0.3 microns
.param l=0.3u

* Input circuit file
.include C:\My_Documents\VLSI\ABopamp3\tspice\single_lp.sp
*.include Z:\VLSI\ABopamp3\tspice\single.sp
* SPICE models
.include C:\My_Documents\VLSI\ABopamp3\tspice\t16w05n.md
*.include Z:\VLSI\ABopamp3\tspice\t16w05n.md
.include C:\My_Documents\VLSI\ABopamp3\tspice\t16w05p.md
*.include Z:\VLSI\ABopamp3\tspice\t16w05p.md

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* Important (Default) Simulation Options
* .options abstol=5e-010 chargetol=1e-014 gmin=0 moscap=0
  * .options relchargetol=reltol reltol=1e-4 vntol=1e-3
  .options abstol=1e-012 chargetol=1e-015 gmin=1e-15 moscap=1
  .options relchargetol=1e-6 reltol=1e-6 vntol=1e-6

* Grid Size and Range for MOS I-V Internal Tables
* To turn off internal tables, set deftables to 0
  .options deftables=0
  .vrange mos 5.5
  .gridsize mos 128 256 64

* DC Power Supplies
VVdd Vdd Gnd 1.5
VVss Vss Gnd 0

* DC Inputs
*v1 v+ gnd 1.5161e-001 AC 1 0
*v2 v- gnd 0.15
*v2 v- v+ 0
* Differential input signals
*v1 vv1 gnd 0
*v2 vcm gnd 0.15
*e1 v+ vcm vv1 gnd 1
*e1 v- vcm gnd vv1 1
I1 ibias vss 100u

*DC sweep analysis settings to measure transconductance
characteristic

*R1 out tp 100
*v3t tp gnd 0.75

*AC analysis settings
*R1 out va- 100Meg
*vac va- v- 0.6
*C1 v- gnd 10u

*Transient Analysis - voltage follower
*Vvin v+ gnd pulse(0.1 0.3 2n 1n 1n 30.25n 62.5n)
*Vvin v+ gnd 0.1 pulse(0.1 0.3 2n 1n 1n 49n 100n)
*Vvin v+ gnd pulse(0.1 0.3 2n 1n 1n 99n 200n)
*Vvin v+ gnd 0.15 pulse(0 0.3 2n 2n 2n 173n 350n)
*Vvin v+ gnd pulse(0.1 0.4 5n 10n 10n 490n 1000n)
*v7 out v- 0.6

*Transient Analysis - inverter
R1i out vb- 300k
C1i out vb- 0.5p
v1i vb- v- 0.6
R2i vin vb- 300k
C2i vin vb- 0.5p
Vvin vin gnd 0.75 pulse(0 1.5 5n 10n 10n 490n 1000n)
*Vvin vin gnd 1.5 pulse(0 1.5 2n 1n 1n 49n 100n)
*Vvin vin gnd pulse(0 1.5 2n 1n 1n 99n 200n)
*Vvin vin gnd pulse(0 1.5 2n 2n 2n 173n 350n)
*Vvin vin gnd pulse(0 2 2n 5n 5n 195n 400n)
v2i v+ gnd 0.15
*Loads
Cload out gnd 20p
Cc x tp1 4p
Rz tp1 out 1.5k

*Measurements
.measure dc voffset find v(v+) when v(out)=0.75 cross=1
.measure dc offset param='voffset-0.15'
.measure dc Itotal find I(Vvss) when V(out)=0.75 cross=1
.measure dc Spower param='1.5*Itotal'
.measure dc x1 when v(out)=1 cross=1
.measure dc x2 when v(out)=0.5 cross=1
.measure dc Aol param='0.5/(x1-x2)' 
.measure dc AoldB param='20*log10(Aol)'
*.measure dc v3 find v(w) at=101.80m
*.measure dc v4 find v(w) at=137.56m
*.measure dc A1 param='(V3-V4)/(137.56m-101.80m)'

*AC measurements
.measure ac p180 find Vp(Out) when Vdb(Out)=0 cross=1
.measure ac PM param='180-abs(p180)'
.measure ac GM find Vdb(Out) when vp(Out)=-178 cross=1
.measure ac AoldB find Vdb(Out) at=50
.measure ac Aol param='10^(AoldB/20)'
.measure ac ft when Vdb(Out)=0 cross=1

*Tran measurements
.measure tran x1 when v(out)=1 cross=1
.measure tran x2 when v(out)=.5 cross=1
.measure tran SRu param='0.5/(x2-x1)'
.measure tran x3 when v(out)=1 cross=2
.measure tran x4 when v(out)=.5 cross=2
.measure tran SRd param='0.5/(x3-x4)'
*Tran measurements - Voltage follower-
.measure tran x1f when v(out)=0.8 cross=1
.measure tran x2f when v(out)=0.7 cross=1
.measure tran SRdf param='abs(0.1/(x2f-x1f))'
.measure tran x3f when v(out)=0.8 cross=2
.measure tran x4f when v(out)=0.7 cross=2
.measure tran SRuf param='abs(0.1/(x3f-x4f))'

* Input Waveforms

*Analysis
.op
*.dc lin v1 0.14 0.16 0.0001
*.dc lin v1 -0.3 0.6 0.0001
*.dc lin v1 0 0.3 0.0001
*.dc lin v1 0 1.5 0.0001
*.ac dec 202 10 10G
.tran/op 5n 2u method=bdf

* Print Results
*.print dc v(out)
*.print dc is(M1) is(M2)
*.print dc is(M6) id(M7) i(R1)
*.print dc is(M1) v(1,2)
*.print ac vdb(out) vp(out)
*.print tran V(out) V(v+) i(Cc) i(Clload) is(M6) id(M7)
.print tran V(out) V(vin) i(Cc) i(Clload) is(M6) id(M7)
A.1.7  Hybrid Op-Amp SPICE Listing (Chapter 3)

* Main circuit: Hybrid, Chapter 3

M5a out1x ib vss vss NMOS L='4*l' W='862*l' AD='862*l*5*l'
  PD='2*l*(862+5)' AS='862*l*5*l' PS='2*l*(862+5)'

M6a out1 ib vss vss NMOS L='4*l' W='862*l' AD='862*l*5*l'
  PD='2*l*(862+5)' AS='862*l*5*l' PS='2*l*(862+5)'

M3 N2 ibias vss vss NMOS L='4*l' W='37*l' AD='37*l*5*l'
  PD='2*l*(37+5)' AS='37*l*5*l' PS='2*l*(37+5)' M=2

M1 ibias ibias vss vss NMOS L='4*l' W='37*l' AD='37*l*5*l'
  PD='2*l*(37+5)' AS='37*l*5*l' PS='2*l*(37+5)' M=2

M7a ib vbias out1x vss NMOS L='4*l' W='75*l' AD='75*l*5*l'
  PD='2*l*(75+5)' AS='75*l*5*l' PS='2*l*(75+5)'

M2 N1 ibias vss vss NMOS L='4*l' W='37*l' AD='37*l*5*l'
  PD='2*l*(37+5)' AS='37*l*5*l' PS='2*l*(37+5)' M=2

Moutn out ib3 vss vss NMOS L='3*l' W='288*l' AD='288*l*5*l'
  PD='2*l*(288+5)' AS='288*l*5*l' PS='2*l*(288+5)'

M8 ib1 ibias vss vss NMOS L='4*l' W='37*l' AD='37*l*5*l'
  PD='2*l*(37+5)' AS='37*l*5*l' PS='2*l*(37+5)' M=2

M9 ib2 ibias vss vss NMOS L='4*l' W='37*l' AD='37*l*5*l'
  PD='2*l*(37+5)' AS='37*l*5*l' PS='2*l*(37+5)' M=2

M8b ib3 ib3 vss vss NMOS L='3*l' W='144*l' AD='144*l*5*l'
  PD='2*l*(144+5)' AS='144*l*5*l' PS='2*l*(144+5)'

M4a N2 vcm 1 1 PMOS L='4*l' W='230*l' AD='230*l*5*l'
  PD='2*l*(230+5)' AS='230*l*5*l' PS='2*l*(230+5)'

M1a out1x v- 1 1 PMOS L='4*l' W='921*l' AD='921*l*5*l'
  PD='2*l*(921+5)' AS='921*l*5*l' PS='2*l*(921+5)'

M2a out1 v+ 1 1 PMOS L='4*l' W='921*l' AD='921*l*5*l'
  PD='2*l*(921+5)' AS='921*l*5*l' PS='2*l*(921+5)'

M3a N2 vdd vdd PMOS L='4*l' W='2763*l' AD='2763*l*5*l'
  PD='2*l*(2763+5)' AS='2763*l*5*l' PS='2*l*(2763+5)'

M4 N1 N1 vdd vdd PMOS L='4*l' W='112*l' AD='112*l*5*l'
  PD='2*l*(112+5)' AS='112*l*5*l' PS='2*l*(112+5)' M=2
M5 out1 N1 vdd vdd PMOS L='4*l' W='112*l' AD='112*l*5*l' PD='2*l'(112+5) AS='112*l*5*l' PS='2*l'(112+5) M=2

M6 ib N1 vdd vdd PMOS L='4*l' W='112*l' AD='112*l*5*l' PD='2*l'(112+5) AS='112*l*5*l' PS='2*l'(112+5) M=2

Moutp out ib2 vdd vdd PMOS L='3*l' W='864*l' AD='864*l*5*l' PD='2*l*(864+5) AS='864*l*5*l' PS='2*l*(864+5)

M1b ib3 out1x 2 2 PMOS L='4*l' W='921*l' AD='921*l*5*l' PD='2*l*(921+5) AS='921*l*5*l' PS='2*l*(921+5)

M4b vss out1 3 3 PMOS L='4*l' W='921*l' AD='921*l*5*l' PD='2*l*(921+5) AS='921*l*5*l' PS='2*l*(921+5)

M2b ib1 out1 2 2 PMOS L='4*l' W='230*l' AD='230*l*5*l' PD='2*l*(230+5) AS='230*l*5*l' PS='2*l*(230+5)

M5b ib2 out1x 3 3 PMOS L='4*l' W='230*l' AD='230*l*5*l' PD='2*l*(230+5) AS='230*l*5*l' PS='2*l*(230+5)

M3b 2 ib1 vdd vdd PMOS L='4*l' W='432*l' AD='432*l*5*l' PD='2*l*(432+5) AS='432*l*5*l' PS='2*l*(432+5)

M7 ib3 N1 vdd vdd PMOS L='4*l' W='112*l' AD='112*l*5*l' PD='2*l*(112+5) AS='112*l*5*l' PS='2*l*(112+5) M=2

M6b 3 ib2 vdd vdd PMOS L='3*l' W='432*l' AD='432*l*5*l' PD='2*l*(432+5) AS='432*l*5*l' PS='2*l*(432+5)

* End of main circuit: Hybrid, Chapter 4

.SUBCKT vcm ibias v1 v2 vcm vdd vss

M8 N3 ibias vss vss NMOS L='4*l' W='108*l' AD='108*l*5*l' PD='2*l*(108+5) AS='108*l*5*l' PS='2*l*(108+5)

M9 vcm ibias vss vss NMOS L='4*l' W='108*l' AD='108*l*5*l' PD='2*l*(108+5) AS='108*l*5*l' PS='2*l*(108+5)

M10 ibias ibias vss vss NMOS L='4*l' W='108*l' AD='108*l*5*l' PD='2*l*(108+5) AS='108*l*5*l' PS='2*l*(108+5)

M1 vss v1 N24 N24 PMOS L='4*l' W='103*l' AD='103*l*5*l' PD='2*l*(103+5) AS='103*l*5*l' PS='2*l*(103+5)

M3 vcm vcm N28 N28 PMOS L='4*l' W='103*l' AD='103*l*5*l' PD='2*l*(103+5) AS='103*l*5*l' PS='2*l*(103+5)

M2 vcm vcm N24 N24 PMOS L='4*l' W='103*l' AD='103*l*5*l' PD='2*l*(103+5) AS='103*l*5*l' PS='2*l*(103+5)

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M4 vss v2 N28 N28 PMOS L='4'*l' W='103*'l' AD='103*'l'*5*'l' PD='2*'l'*(103+5)' AS='103*'l'*5*'l' PS='2*'l'*(103+5)'
M5 N24 N3 vdd vdd PMOS L='4'*l' W='207*'l' AD='207*'l'*5*'l' PD='2*'l'*(207+5)' AS='207*'l'*5*'l' PS='2*'l'*(207+5)'
M6 N28 N3 vdd vdd PMOS L='4'*l' W='207*'l' AD='207*'l'*5*'l' PD='2*'l'*(207+5)' AS='207*'l'*5*'l' PS='2*'l'*(207+5)'
M7 N3 N3 vdd vdd PMOS L='4'*l' W='207*'l' AD='207*'l'*5*'l' PD='2*'l'*(207+5)' AS='207*'l'*5*'l' PS='2*'l'*(207+5)'
.ENDS

* Lambda (l) is 0.3 microns
.param l=0.3u

* Input circuit file
.include C:\My_Documents\VLSI\ABopamp3\tspice\hybrid4.sp
*.include Z:\VLSI\ABopamp3\tspice\sabout.sp

* SPICE models
.include C:\My_Documents\VLSI\ABopamp3\tspice\t16w05n.md
*.include Z:\VLSI\ABopamp3\tspice\t16w05n.md
.include C:\My_Documents\VLSI\ABopamp3\tspice\t16w05p.md
*.include Z:\VLSI\ABopamp3\tspice\t16w05p.md

* Important (Default) Simulation Options
* .options abstol=5e-010 chargetol=1e-014 gmin=0 moscap=0
* .options relchargetol=reltol reltol=1e-4 vntol=1e-3
.options abstol=1e-012 chargetol=1e-015 gmin=1e-15 moscap=1
.options relchargetol=1e-6 reltol=1e-6 vntol=1e-6

* Grid Size and Range for MOS I-V Internal Tables
* To turn off internal tables, set deftables to 0
.options deftables=0
.vrange mos 5.5
.gridsize mos 128 256 64

* DC Power Supplies
VVdd Vdd Gnd 1.5
VVss Vss Gnd 0

* DC Inputs
*v1 v+ gnd 1.5077e-001 AC 1 0
*v2 v- gnd 0.15
*v2 v- v+ 0

* Differential input signals
*v1 vv1 gnd 0
*v2 vcm gnd 0.15
*e1 v+ vcm vv1 gnd 1
*e1 v- vcm gnd vv1 1
I1 vdd ibias 25u
v6 vbias gnd 1.2
*v7 vbias2 gnd 1.3
I2 vdd ibias2 10u

* DC sweep analysis settings to measure transconductance characteristic
*R1 out tp 100
*v3t tp gnd 0.75

* AC analysis settings
*R1a out va- 100Meg
*v7a va- v- 0.6
*C1a v- gnd 10u

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*Transient Analysis
*Vvin v+ gnd pulse(0.1 0.3 2n 1n 1n 30.25n 62.5n)
*Vvin v+ gnd pulse(0.1 0.3 2n 1n 1n 49n 100n)
*Vvin v+ gnd pulse(0.1 0.3 2n 1n 1n 99n 200n)
*Vvin v+ gnd pulse(0.1 0.4 5n 10n 10n 490n 1000n)
*v7 v- out 0

*Transient Analysis - inverter
R1i out vb- 300k
C1i out vb- 0.5p
v1i vb- v- 0.6
R2i vin vb- 300k
C2i vin vb- 0.5p
*Vvin vin gnd pulse(0 1.5 2n 1n 1n 49n 100n)
Vvin vin gnd 0.75 pulse(0 1.5 2n 2n 2n 173n 350n)
*Vvin vin gnd pulse(0 1.5 2n 2n 2n 348n 700n)
*Vvin vin gnd 0.75 pulse(0 1.5 2n 5n 5n 495n 1000n)
v2i v+ gnd 0.15

*Loads
Cload out gnd 20p
Cc out1 tp1 16p
Rz tp1 out 900
*.param C=0.1p
*Cc2 ib2 gnd 'C'
*Measurements
.measure dc voffset1 find v(v+) when v(out)=0.75 cross=1
.measure dc Itotal find I(Vvss) when V(out)=0.75 cross=1
.measure dc Spower param='1.5*Itotal'

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.measure dc x1 when v(out)=1 cross=1
.measure dc x2 when v(out)=0.5 cross=1
.measure dc Aol param='0.5/(x1-x2)'
.measure dc AoldB param='20*log10(Aol)'
.measure dc p1 find is(moutp) at=0.1
.measure dc p2 find id(moutn) at=0.2
*AC measurements
.measure ac p180 find Vp(Out) when Vdb(Out)=0 cross=1
.measure ac PM param='180-abs(p180)'
.measure ac GM find Vdb(Out) when vp(Out)=-178 cross=1
.measure ac AoldB find Vdb(Out) at=50
.measure ac Aol param='10^(AoldB/20)'
.measure ac ft when Vdb(Out)=0 cross=1
*Tran measurements
.measure tran x1 when v(out)=1 cross=1
.measure tran x2 when v(out)=.5 cross=1
.measure tran SRd param='0.5/(x2-x1)'
.measure tran x3 when v(out)=1 cross=2
.measure tran x4 when v(out)=.5 cross=2
.measure tran SRu param='0.5/(x3-x4)'

* Input Waveforms

*Analysis
.op
*.dc lin v1 0.14 0.16 0.0001
*.dc lin v1 0 0.3 0.0001
*.dc lin v1 0 0.3 0.0001 sweep lin var 1.1 1.5 0.1
*.dc lin v1 0 0.3 0.0001
*.dc lin v1 0 1.5 0.0001

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A.1.8 Hybrid Op-Amp SPICE Listing (Chapter 4)

* Main circuit: Hybrid, Chapter 4
M8 ibias ibias vss vss NMOS W='16*l' L='5*l' AS='16*5*l*l' AD='16*5*l*l' PS='2*(16+5)*l' PD='2*(16+5)*l' M=2
XP_1 vo1+ vo1- Out vbias2 vdd ibias vss Gnd Peluso2
XR_1 ibias2 V+ V- vo1+ vo1- vbias vdd ibias vss Gnd Ramirez1
* End of main circuit: Hybrid, Chapter 4

.SUBCKT Peluso2 In+ In- Out vbias Vdd vgate Vss Gnd
M1 Gnd In+ N3 Vdd PMOS L='5*l' W='28*l' AD='28*5*l*l' PD='2*(28+5)*l' AS='28*5*l*l' PS='2*(28+5)*l' M=12
M5 N3 1 Vdd Vdd PMOS L='5*l' W='28*l' AD='28*5*l*l' PD='2*(28+5)*l'
AS='28*5*I'* I' PS='2*(28+5)*I' M=36
M4 2 In+ N6 Vdd PMOS L='5*I' W='28*I' AD='28*5*I'* I' PD='2*(28+5)*I'
AS='28*5*I'* I' PS='2*(28+5)*I' M=12
M2 1 In- N3 Vdd PMOS L='5*I' W='28*I' AD='28*5*I'* I' PD='2*(28+5)*I'
AS='28*5*I'* I' PS='2*(28+5)*I' M=12
M3 N8 In- N6 Vdd PMOS L='5*I' W='28*I' AD='28*5*I'* I' PD='2*(28+5)*I'
AS='28*5*I'* I' PS='2*(28+5)*I' M=12
M6 N6 2 Vdd Vdd PMOS L='5*I' W='28*I' AD='28*5*I'* I' PD='2*(28+5)*I'
AS='28*5*I'* I' PS='2*(28+5)*I' M=36
M12 Out 1 Vdd Vdd PMOS L='3*I' W='84*I' AD='84*5*I'* I'
PD='2*(84+5)*I' AS='84*5*I'* I' PS='2*(84+5)*I' M=36
M15 N5 N5 Vdd Vdd PMOS L='5*I' W='32*I' AD='32*5*I'* I'
PD='2*(32+5)*I' AS='32*5*I'* I' PS='2*(32+5)*I' M=2
M14 N1 N5 Vdd Vdd PMOS L='5*I' W='32*I' AD='32*5*I'* I'
PD='2*(32+5)*I' AS='32*5*I'* I' PS='2*(32+5)*I' M=2
M16 N5 vgate Vss Vss NMOS W='16*I' L='5*I' AS='16*5*I'* I'
AD='16*5*I'* I' PD='2*(16+5)*I' M=2
M8 2 vgate Vss Vss NMOS W='16*I' L='5*I' AS='16*5*I'* I' AD='16*5*I'* I'
PD='2*(16+5)*I' M=2
M7 1 vgate Vss Vss NMOS W='16*I' L='5*I' AS='16*5*I'* I' AD='16*5*I'* I'
PD='2*(16+5)*I' M=2
M11 Out N1 Vss Vss NMOS W='10*I' L='3*I' AS='10*5*I'* I' AD='10*5*I'* I'
PS='2*(10+5)*I' PD='2*(10+5)*I' M=36
M10 N8 N1 Vss Vss NMOS W='10*I' L='5*I' AS='10*5*I'* I' AD='10*5*I'* I'
PS='2*(10+5)*I' PD='2*(10+5)*I' M=12
M13 N1 vbias N8 Vss NMOS W='10*I' L='5*I' AS='10*5*I'* I'
AD='10*5*I'* I' PD='2*(10+5)*I' M=12
.ENDS

.SUBCKT vcm ibias In+ In- vcm Vdd Vss Gnd
M14 vcm vcm N1 Vdd PMOS L='5*I' W='12*I' AD='12*5*I'* I'
PD='2*(12+5)*I' AS='12*5*I'* I' PS='2*(12+5)*I' M=3
M15 Gnd In- N1 Vdd PMOS L='5*I' W='12*I' AD='12*5*I'* I'
PD='2*(12+5)*I' AS='12*5*I'* I' PS='2*(12+5)*I' M=3
M12 Gnd In+ N8 Vdd PMOS L='5*I' W='12*I' AD='12*5*I'* I'

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PD='2*(12+5)*l' AS='12*5*l*l' PS='2*(12+5)*l' M=3
M13 vcm vcm N8 Vdd PMOS L='5*l' W='12*l' AD='12*5*l*l'
PD='2*(12+5)*l' AS='12*5*l*l' PS='2*(12+5)*l' M=3
M10 N1 N24 Vdd Vdd PMOS L='5*l' W='21*l' AD='21*5*l*l'
PD='2*(21+5)*l' AS='21*5*l*l' PS='2*(21+5)*l' M=4
M9 N8 N24 Vdd Vdd PMOS L='5*l' W='21*l' AD='21*5*l*l'
PD='2*(21+5)*l' AS='21*5*l*l' PS='2*(21+5)*l' M=4
M11 N24 N24 Vdd Vdd PMOS L='5*l' W='21*l' AD='21*5*l*l'
PD='2*(21+5)*l' AS='21*5*l*l' PS='2*(21+5)*l' M=4
M17 vcm ibias Vss Vss NMOS W='7*l' L='5*l' AS='7*5*l*l' AD='7*5*l*l'
PS='2*(7+5)*l' PD='2*(7+5)*l' M=4
M18 N24 ibias Vss Vss NMOS W='7*l' L='5*l' AS='7*5*l*l' AD='7*5*l*l'
PS='2*(7+5)*l' PD='2*(7+5)*l' M=4
M16 ibias ibias Vss Vss NMOS W='7*l' L='5*l' AS='7*5*l*l' AD='7*5*l*l'
PS='2*(7+5)*l' PD='2*(7+5)*l' M=4
.ENDS

.SUBCKT Ramirez1 ibias In+ In- Out+ Out- vbias Vdd vgate Vss Gnd
M1 Out- In- low Vdd PMOS L='5*l' W='28*l' AD='28*5*l*l'
PD='2*(28+5)*l' AS='28*5*l*l' PS='2*(28+5)*l' M=12
M3 low 4sync Vdd Vdd PMOS L='5*l' W='28*l' AD='28*5*l*l'
PD='2*(28+5)*l' AS='28*5*l*l' PS='2*(28+5)*l' M=36
M11 pbias pbias Vdd Vdd PMOS L='5*l' W='32*l' AD='32*5*l*l'
PD='2*(32+5)*l' AS='32*5*l*l' PS='2*(32+5)*l' M=2
M2 Out+ In+ low Vdd PMOS L='5*l' W='28*l' AD='28*5*l*l'
PD='2*(28+5)*l' AS='28*5*l*l' PS='2*(28+5)*l' M=12
M4 4sync vcm low Vdd PMOS L='5*l' W='28*l' AD='28*5*l*l'
PD='2*(28+5)*l' AS='28*5*l*l' PS='2*(28+5)*l' M=12
M12 ngate pbias Vdd Vdd PMOS L='5*l' W='32*l' AD='32*5*l*l'
PD='2*(32+5)*l' AS='32*5*l*l' PS='2*(32+5)*l' M=2
M13 Out+ pbias Vdd Vdd PMOS L='5*l' W='32*l' AD='32*5*l*l'
PD='2*(32+5)*l' AS='32*5*l*l' PS='2*(32+5)*l' M=2
M5 Out- ngate Vss Vss NMOS W='10*l' L='5*l' AS='10*5*l*l'
AD='10*5*l*l' PS='2*(10+5)*l' PD='2*(10+5)*l' M=12
M9 pbias vgate Vss Vss NMOS W='16*l' L='5*l' AS='16*5*l*l'
AD='16*5*l*l' PS='2*(16+5)*l' PD='2*(16+5)*l' M=2

M7 ngate vbias Out- Vss NMOS W='10*l' L='5*l' AS='10*5*l*l'
AD='10*5*l*l' PS='2*(10+5)*l' PD='2*(10+5)*l' M=12

M6 Out+ ngate Vss Vss NMOS W='10*l' L='5*l' AS='10*5*l*l'
AD='10*5*l*l' PS='2*(10+5)*l' PD='2*(10+5)*l' M=12

M10 4sync vg ate Vss Vss NMOS W='16*l' L='5*l' AS='16*5*l*l'
AD='16*5*l*l' PS='2*(16+5)*l' PD='2*(16+5)*l' M=2

Xvcm_1 ibias In+ In- vcm Vdd Vss Gnd vcm

.ENDS

* Lambda (l) is 0.3 microns
.param l=0.3u

* Input circuit file
*.include Z:\VLSI\ABopamp2\t-spice\RP.sp
*.include H:\VLSI\ABopamp2\l-edit\RP.spc
.include C:\My_Documents\VLSI\ABopamp2\t-spice\RP.sp
*.include C:\My_Documents\VLSI\ABopamp2\l-edit\RP.spc

* SPICE models
*.include Z:\VLSI\ABopamp2\t-spice\t16w05p.md
.include C:\My_Documents\VLSI\ABopamp2\t-spice\t16w05n.md
*.include Z:\VLSI\ABopamp2\t-spice\t16w05n.md
.include C:\My_Documents\VLSI\ABopamp2\t-spice\t16w05p.md

* Important (Default) Simulation Options
* .options abstol=5e-010 chargetol=1e-014 gmin=0 moscap=0
* .options relchargetol=reltol reltol=1e-4 vntol=1e-3
.options abstol=1e-012 chargetol=1e-015 gmin=1e-15 moscap=1
.options relchargetol=1e-6 reltol=1e-6 vntol=1e-6

* Grid Size and Range for MOS I-V Internal Tables

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* To turn off internal tables, set deftables to 0
   .options deftables=0
   .vrang mos 5.5
   .gridsize mos 128 256 64

* DC Power Supplies
VVdd Vdd Gnd 1.5
VVss Vss Gnd 0

* DC Inputs
**DC AND AC ANALYSIS SETUP
v1 v+ Gnd 1.2761e-001 AC 1 0
*v2 v- Gnd 0.125

I1 Vdd ibias2 0.8u
I2 Vdd ibias 3u
v4 vbias Gnd 1.1
v5 vbias2 Gnd 1.3

*DC sweep analysis settings to measure transconductance characteristic
*R2 out tp 100
*v3t tp gnd 0.75

*AC analysis settings
R1a out va- 100Meg
v7a va- v- 0.625
C1a v- gnd 10u

*Transient Analysis - voltage follower
*Vvin v+ gnd pulse(0.1 0.3 5n 10n 10n 490n 1000n)
*Vvin in+ gnd pulse(0.1 0.5 5n 0.05u 0.05u 1.2u 2.5u)
*Vvin v+ gnd pulse(0.1 0.3 5n 0.1u 0.1u 4.9u 10u)
*Vvin v+ gnd pulse(0.1 0.3 5n 0.1u 0.1u 49.9u 100u)
*v7 in- out 0

*Transient Analysis - voltage inverter
*R1i out vb- 100k
*C1i out vb- 0.1p
*v1i vb- v- 0.625
*R2i vin vb- 100k
*C2i vin vb- 0.1p
*Vvin vin gnd pulse(0 1.5 5n 0.01u 0.01u 2.49u 5u)
*Vvin vin gnd pulse(0 1.5 5n 0.02u 0.02u 1.23u 2.5u)
*Vvin vin gnd 0
*Vvin vin gnd pulse(0 1.5 5n 0.1u 0.1u 4.9u 10u)
*Vvin vin gnd pulse(0 1.5 5n 0.1u 0.1u 49.9u 100u)
*v2i v+ gnd 0.125

**COMPENSATION CIRCUITRY TO BE USED WITH *.SP
Rz vo1+ vint 6k
Cc vint Out 3.2p
cload Out Gnd 20p
Rload Out Gnd 10Meg

*Measurements
.measure dc voffset1 find v(v+) when v(out)=0.75 cross=1
.measure dc offset param='voffset1-0.125'
.measure dc Itotal find I(Vvss) when V(out)=0.75 cross=1
.measure dc Spower param='1.5*Itotal'

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.measure dc x1 when v(out)=1 cross=1
.measure dc x2 when v(out)=0.5 cross=1
.measure dc Aol param='0.5/(x1-x2)'
*.measure dc AoldB param='20*log10(Aol)'
*AC measurements
.measure ac p180 find Vp(Out) when Vdb(Out)=0 cross=1
.measure ac PM param='180-abs(p180)'
.measure ac GM find Vdb(Out) when vp(Out)=-178 cross=1
.measure ac AoldB find Vdb(Out) at=50
.measure ac Aol param='10^(AoldB/20)'
.measure ac ft when Vdb(Out)=0 cross=1
*Tran measurements
.measure tran x1 when v(out)=1.2 cross=1
.measure tran x2 when v(out)=.7 cross=1
.measure tran SRd param='0.5/(x2-x1)'
.measure tran x3 when v(out)=1.2 cross=2
.measure tran x4 when v(out)=.7 cross=2
.measure tran SRu param='0.5/(x3-x4)'
*Tran measurements -voltage follower
*.measure tran x1 when v(RP_out)=0.25 cross=1
*.measure tran x2 when v(RP_out)=.15 cross=1
*.measure tran SRu param='0.1/(x1-x2)'
*.measure tran x3 when v(RP_out)=0.25 cross=2
*.measure tran x4 when v(RP_out)=.15 cross=2
*.measure tran SRd param='0.1/(x4-x3)'
* Input Waveforms

*Analysis
.op
*.dc lin v1 0.117 0.135 0.0001
* .dc lin Vvin 0 1.5 5.95e-3
  .ac dec 101 10 10g
  *.tran/op 5n 500n method=bdf
  *.tran/op 500n 100u method=bdf
  *.tran/op 500n 50u method=bdf
  *.tran/op 50u 500u method=bdf
  *.tran/op 50u 2.5u method=bdf
  *.tran/op 50n 10u method=bdf
  *.tran/op 50u 5m method=bdf
  *.options prtdel=9.92e-9

  * Print Results
  * .print dc v(Out)
  * .print dc i(XP_1.M11) i(XP_1.M12) i(R2)
  * .print dc i(M140) i(M130) i(R2)
  .print ac vdb(Out) vp(Out)
  * .print tran i(XP_1.M11) i(XP_1.M12) i(Cc) i(Cload)
  * .print tran v(vin) v(out)

A.1.9 Hybrid-2 Op-Amp SPICE Listing

* Main circuit: Hybrid-2

  M8 ibias ibias vss vss NMOS W='16*l' L='5*l' AS='16*5*l*l' AD='16*5*l*l' PS='2*(16+5)*l' PD='2*(16+5)*l' M=2
  XP_1 v+ v- vo1+ vo1- vbias1 vdd ibias vss Peluso1
  XP_2 vo1+ vo1- Out vbias2 vdd ibias vss Gnd Peluso2

* End of main circuit: Hybrid-2
.SUBCKT Peluso1 In+ In- Out+ Out- vbias Vdd vgate Vss
M1 Out- In- N17 Vdd PMOS L='5*l' W='28*l' AD='28*5*l' I' PD='2*(28+5)*I' AS='28*5*l' I' PS='2*(28+5)*I' M=12
M5 N17 ib1 Vdd PMOS L='5*l' W='28*l' AD='28*5*l' I' PD='2*(28+5)*I' AS='28*5*l' I' PS='2*(28+5)*I' M=36
M4 ib2 In- N13 Vdd PMOS L='5*l' W='28*l' AD='28*5*l' I' PD='2*(28+5)*I' AS='28*5*l' I' PS='2*(28+5)*I' M=12
M2 ib1 In+ N17 Vdd PMOS L='5*l' W='28*l' AD='28*5*l' I' PD='2*(28+5)*I' AS='28*5*l' I' PS='2*(28+5)*I' M=12
M3 Out+ In+ N13 Vdd PMOS L='5*l' W='28*l' AD='28*5*l' I' PD='2*(28+5)*I' AS='28*5*l' I' PS='2*(28+5)*I' M=12
M6 N13 ib2 Vdd PMOS L='5*l' W='28*l' AD='28*5*l' I' PD='2*(28+5)*I' AS='28*5*l' I' PS='2*(28+5)*I' M=36
M18 Out+ N1 Vdd PMOS L='5*l' W='32*l' AD='32*5*l' I' PD='2*(32+5)*I' AS='32*5*l' I' PS='2*(32+5)*I' M=2
M15 N1 N1 Vdd PMOS L='5*l' W='32*l' AD='32*5*l' I' PD='2*(32+5)*I' AS='32*5*l' I' PS='2*(32+5)*I' M=2
M14 ib3 N1 Vdd PMOS L='5*l' W='32*l' AD='32*5*l' I' PD='2*(32+5)*I' AS='32*5*l' I' PS='2*(32+5)*I' M=2
M16 N1 vgate Vss NMOS W='16*l' L='5*l' AD='16*5*l' I' PS='2*(16+5)*I' PD='2*(16+5)*I' M=2
M8 ib1 vgate Vss NMOS W='16*l' L='5*l' AD='16*5*l' I' PS='2*(16+5)*I' PD='2*(16+5)*I' M=2
M7 ib2 vgate Vss NMOS W='16*l' L='5*l' AD='16*5*l' I' PS='2*(16+5)*I' PD='2*(16+5)*I' M=2
M11 Out+ ib3 Vss NMOS W='10*l' L='5*l' AD='10*5*l' I' PS='2*(10+5)*I' PD='2*(10+5)*I' M=12
M10 Out- ib3 Vss NMOS W='10*l' L='5*l' AD='10*5*l' I' PS='2*(10+5)*I' PD='2*(10+5)*I' M=12
M13 ib3 vbias Out- Vss NMOS W='10*l' L='5*l' AD='10*5*l' I' PS='2*(10+5)*I' PD='2*(10+5)*I' M=12
.ENDS

.SUBCKT Peluso2 In+ In- Out vbias Vdd vgate Vss Gnd
M1 Gnd In+ N3 Vdd PMOS L='5*l' W='28*l' AD='28*5*l' I'
PD='2*(28+5)*l' AS='28*5*l*l' PS='2*(28+5)*l' M=12
M5 N3 1 Vdd Vdd PMOS L='5*l' W='28*l' AD='28*5*l*l' PD='2*(28+5)*l'
AS='28*5*l*l' PS='2*(28+5)*l' M=36
M4 2 In+ N6 Vdd PMOS L='5*l' W='28*l' AD='28*5*l*l' PD='2*(28+5)*l'
AS='28*5*l*l' PS='2*(28+5)*l' M=12
M2 1 In- N3 Vdd PMOS L='5*l' W='28*l' AD='28*5*l*l' PD='2*(28+5)*l'
AS='28*5*l*l' PS='2*(28+5)*l' M=12
M3 N8 In- N6 Vdd PMOS L='5*l' W='28*l' AD='28*5*l*l' PD='2*(28+5)*l'
AS='28*5*l*l' PS='2*(28+5)*l' M=12
M6 N6 2 Vdd Vdd PMOS L='5*l' W='28*l' AD='28*5*l*l' PD='2*(28+5)*l'
AS='28*5*l*l' PS='2*(28+5)*l' M=36
M12 Out 1 Vdd Vdd PMOS L='3*l' W='84*l' AD='84*5*l*l'
PD='2*(84+5)*l' AS='84*5*l*l' PS='2*(84+5)*l' M=36
M15 N5 N5 Vdd Vdd PMOS L='5*l' W='32*l' AD='32*5*l*l'
PD='2*(32+5)*l' AS='32*5*l*l' PS='2*(32+5)*l' M=2
M14 N1 N5 Vdd Vdd PMOS L='5*l' W='32*l' AD='32*5*l*l'
PD='2*(32+5)*l' AS='32*5*l*l' PS='2*(32+5)*l' M=2
M16 N5 vgate Vss Vss NMOS W='16*l' L='5*l' AS='16*5*l*l'
AD='16*5*l*l' PS='2*(16+5)*l' PD='2*(16+5)*l' M=2
M8 2 vgate Vss Vss NMOS W='16*l' L='5*l' AS='16*5*l*l' AD='16*5*l*l'
PD='2*(16+5)*l' PS='2*(16+5)*l' M=2
M7 1 vgate Vss Vss NMOS W='16*l' L='5*l' AS='16*5*l*l' AD='16*5*l*l'
PD='2*(16+5)*l' PS='2*(16+5)*l' M=2
M11 Out N1 Vss Vss NMOS W='10*l' L='3*l' AS='10*5*l*l' AD='10*5*l*l'
PD='2*(10+5)*l' PS='2*(10+5)*l' M=36
M10 N8 N1 Vss Vss NMOS W='10*l' L='5*l' AS='10*5*l*l' AD='10*5*l*l'
PD='2*(10+5)*l' PS='2*(10+5)*l' M=12
M13 N1 vbias N8 Vss NMOS W='10*l' L='5*l' AS='10*5*l*l'
AD='10*5*l*l' PS='2*(10+5)*l' PD='2*(10+5)*l' M=12
.ENDS
* Lambda (l) is 0.3 microns
.param l=0.3u

* Input circuit file
**TRANSIENT SETUP**

*v2 V- Out 0

I1 Vdd ibias 3u
v4 vbias1 Gnd 1.1
v5 vbias2 Gnd 1.3

* Loads
**COMPENSATION CIRCUITRY TO BE USED WITH *.SP**
Rz vo1+ v 2k
Cc v Out 8p
*Cc1 a vo1+ 0.5p

**AC ANALYSIS SETUP**
c2 v- Gnd 10
v1a va- v- 0.6
R1 Out va- 100Meg

**DC ANALYSIS SETUP - Current measurements**
*R2 Out vt 100
*v3 vt Gnd 0.75

** CAPACITIVE LOAD**
Cload Out Gnd 20p
Rload Out Gnd 10Meg

*Transient Analysis - voltage follower
*Vvin v+ gnd pulse(0.1 0.3 5n 10n 10n 490n 1000n)
*Vvin in+ gnd pulse(0.1 0.5 5n 0.05u 0.05u 1.2u 2.5u)
*Vvin v+ gnd pulse(0.1 0.3 5n 0.1u 0.1u 4.9u 10u)
*Vvin v+ gnd pulse(0.1 0.3 5n 0.1u 0.1u 49.9u 100u)
*v7 in- out 0
*Transient Analysis - voltage inverter

*R1i out vb- 100k
*C1i out vb- 0.1p
*v1i vb- v- 0.625
*R2i vin vb- 100k
*C2i vin vb- 0.1p

*Vvin vin gnd pulse(0 1.5 5n 0.01u 0.01u 2.49u 5u)
*Vvin vin gnd 0
*Vvin vin gnd pulse(0 1.5 5n 0.02u 0.02u 1.23u 2.5u)
*Vvin vin gnd pulse(0 1.5 5n 0.1u 0.1u 4.9u 10u)
*Vvin vin gnd pulse(0 1.5 5n 0.1u 0.1u 49.9u 100u)
*v2i v+ gnd 0.125

*Measurements
.measure dc voffset1 find v(v+) when v(out)=0.75 cross=1
.measure dc offset param='voffset1-0.125'
.measure dc Itotal find I(Vvss) when V(out)=0.75 cross=1
.measure dc Spower param='1.5*Itotal'
.measure dc x1 when v(out)=1 cross=1
.measure dc x2 when v(out)=0.5 cross=1
.measure dc Aol param='0.5/(x1-x2)'
*.measure dc AoldB param='20*log10(Aol)'

*AC measurements
.measure ac p180 find Vp(Out) when Vdb(Out)=0 cross=1
.measure ac PM param='180-abs(p180)'
.measure ac GM find Vdb(Out) when vp(Out)=-178 cross=1
.measure ac AoldB find Vdb(Out) at=50
.measure ac Aol param='10^(AoldB/20)'
.measure ac ft when Vdb(Out)=0 cross=1

*Tran measurements
.measure tran x1 when v(out)=1.2 cross=1
.measure tran x2 when v(out)=.7 cross=1
.measure tran SRd param='0.5/(x2-x1)'
.measure tran x3 when v(out)=1.2 cross=2
.measure tran x4 when v(out)=.7 cross=2
.measure tran SRu param='0.5/(x3-x4)'
*Tran measurements -voltage follower
*.measure tran x1 when v(RP_out)=0.25 cross=1
*.measure tran x2 when v(RP_out)=.15 cross=1
*.measure tran SRu param='0.1/(x1-x2)'
*.measure tran x3 when v(RP_out)=0.25 cross=2
*.measure tran x4 when v(RP_out)=.15 cross=2
*.measure tran SRd param='0.1/(x4-x3)'

*Analysis
.op
**DC ANALYSIS SETUP
*.dc lin v1 0.11 0.14 0.0001
*.dc lin Vvin 0 1.5 5.95e-3
**AC ANALYSIS SETUP
.ac dec 101 10 10g
**Tran ANALYSIS SETUP
*.tran/op 5n 500n method=bdf
*.tran/op 500n 100u method=bdf
*.tran/op 500n 50u method=bdf
*.tran/op 50u 500u method=bdf
*.tran/op 50n 5u method=bdf
*.tran/op 50n 2.5u method=bdf
*.tran/op 50n 10u method=bdf
*.tran/op 50u 5m method=bdf
*.options prtdel=9.92e-9

* Print Results
**DC PRINT RESULT
*.print dc v(Out)
*.print dc i(XP_2.M12) i(XP_2.M11) i(R2)

**AC PRINT RESULT
.print ac vdb(Out) vp(Out)

**Tran PRINT RESULT
*.print tran v(vin) v(Out) i(Cc) i(Cload) i(XP_2.M12) i(XP_2.M11)
B MANUFACTURED CHIP PINOUTS

B.1 Full-AB Op-Amp

Project Author: Carlos Nieva Lozano.

Submitted: March 27, 2001.

Fabrication: 0.5 \( \mu \)m AMI n-well process.

Description: Pin description is shown in Table B.1. Figure B.1 shows the bias setup for Full-AB op-amp. This chip pinout corresponds to the Full-AB op-amp tested in laboratory and described in Chapter 4, section 4.2.

![Figure B.1 Full-AB bias setup.](image-url)
<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Pad Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; Pad</td>
<td>Protect</td>
<td>N-well contact (V&lt;sub&gt;DD&lt;/sub&gt;).</td>
</tr>
<tr>
<td>6</td>
<td>Source/Drain</td>
<td>Protect</td>
<td>Op-amp output.</td>
</tr>
<tr>
<td>7</td>
<td>Gate</td>
<td>Protect</td>
<td>Op-amp negative input (V-).</td>
</tr>
<tr>
<td>8</td>
<td>Gate</td>
<td>Protect</td>
<td>Op-amp positive input (V+).</td>
</tr>
<tr>
<td>9</td>
<td>Drain</td>
<td>Protect</td>
<td>Drain of PMOS Current Mirror.</td>
</tr>
<tr>
<td>21</td>
<td>V&lt;sub&gt;SS&lt;/sub&gt; Pad</td>
<td>Protect</td>
<td>P-substrate (V&lt;sub&gt;SS&lt;/sub&gt;).</td>
</tr>
<tr>
<td>22</td>
<td>Gate</td>
<td>Protect</td>
<td>Gate of NMOS in Cascoded Current Mirror.</td>
</tr>
<tr>
<td>23</td>
<td>Drain</td>
<td>Protect</td>
<td>Drain of NMOS Current Mirror.</td>
</tr>
<tr>
<td>24</td>
<td>Gate</td>
<td>Protect</td>
<td>Gate of PMOS in Cascoded Current Mirror.</td>
</tr>
<tr>
<td>25</td>
<td>Drain</td>
<td>Protect</td>
<td>Drain of PMOS Current Mirror.</td>
</tr>
<tr>
<td>26</td>
<td>Gate</td>
<td>Protect</td>
<td>Gate of NMOS in Cascoded Current Mirror.</td>
</tr>
<tr>
<td>27</td>
<td>Drain</td>
<td>Protect</td>
<td>Drain of NMOS Current Mirror.</td>
</tr>
<tr>
<td>28</td>
<td>Drain</td>
<td>Protect</td>
<td>Drain of NMOS Current Mirror.</td>
</tr>
<tr>
<td>29</td>
<td>Drain</td>
<td>Protect</td>
<td>Drain of NMOS Current Mirror.</td>
</tr>
<tr>
<td>30</td>
<td>Drain</td>
<td>Protect</td>
<td>Drain of PMOS Current Mirror.</td>
</tr>
</tbody>
</table>

Table B.1 Full-AB Op-amp pin description.
B.2 Hybrid and Hybrid-2 Op-Amp

Project Author: Carlos Nieva Lozano.


Fabrication: 0.5 µm AMI n-well process.

Description: Pin descriptions for Hybrid and Hybrid-2 op-amps are shown in Tables B.2 and B.3. Figure B.2 shows the bias setup for Hybrid and Hybrid-2 op-amps. The chip pinouts corresponds to the Hybrid and Hybrid-2 op-amps tested in laboratory and described in Chapter 4, section 4.2.

![Figure B.2 Hybrid and Hybrid 2 op-amp bias setup.](image-url)
<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Pad Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_{DD}$ Pad</td>
<td>Protect</td>
<td>N-well contact ($V_{DD}$).</td>
</tr>
<tr>
<td>21</td>
<td>$V_{SS}$ Pad</td>
<td>Protect</td>
<td>P-substrate ($V_{SS}$).</td>
</tr>
<tr>
<td>24</td>
<td>Drain</td>
<td>Protect</td>
<td>Drain of PMOS</td>
</tr>
<tr>
<td>26</td>
<td>Gate</td>
<td>Protect</td>
<td>Op-amp positive input ($V^+$).</td>
</tr>
<tr>
<td>27</td>
<td>Gate</td>
<td>Protect</td>
<td>Op-amp positive input ($V^-$).</td>
</tr>
<tr>
<td>28</td>
<td>Drain</td>
<td>Protect</td>
<td>Drain of NMOS Current Mirror.</td>
</tr>
<tr>
<td>29</td>
<td>Gate</td>
<td>Protect</td>
<td>Gate of NMOS in Cascoded Current Mirror.</td>
</tr>
<tr>
<td>30</td>
<td>Drain</td>
<td>Protect</td>
<td>Drain of NMOS Current Mirror.</td>
</tr>
<tr>
<td>31</td>
<td>Gate</td>
<td>Protect</td>
<td>Gate of NMOS in Cascoded Current Mirror.</td>
</tr>
<tr>
<td>32</td>
<td>Source/Drain</td>
<td>Bare</td>
<td>Op-amp output.</td>
</tr>
</tbody>
</table>

Table B.2 Hybrid Op-amp pin description.
<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Pad Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_{DD}$ Pad</td>
<td>Protect</td>
<td>N-well contact ($V_{DD}$).</td>
</tr>
<tr>
<td>3</td>
<td>Source/Drain</td>
<td>Bare</td>
<td>Op-amp output.</td>
</tr>
<tr>
<td>16</td>
<td>Gate</td>
<td>Protect</td>
<td>Op-amp positive input ($V^+$).</td>
</tr>
<tr>
<td>17</td>
<td>Gate</td>
<td>Protect</td>
<td>Op-amp positive input ($V^-$).</td>
</tr>
<tr>
<td>18</td>
<td>Gate</td>
<td>Protect</td>
<td>Gate of NMOS in Cascoded Current Mirror.</td>
</tr>
<tr>
<td>19</td>
<td>Gate</td>
<td>Protect</td>
<td>Gate of NMOS in Cascoded Current Mirror.</td>
</tr>
<tr>
<td>20</td>
<td>Drain</td>
<td>Protect</td>
<td>Drain of NMOS Current Mirror.</td>
</tr>
<tr>
<td>21</td>
<td>$V_{SS}$ Pad</td>
<td>Protect</td>
<td>P-substrate ($V_{SS}$).</td>
</tr>
</tbody>
</table>

Table B.3 Hybrid-2 Op-amp pin description.
LITERATURE CITED


[Ram00] J. Ramírez-Angulo, A. Torralba, R. G. Carvajal and J. Tombs, “Low-Voltage CMOS Operational Amplifiers with Wide Input-


